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THIRD QUARTERLY PROGRESS REPORT

Period:
31 OCTOBER 1962 - 31 JANUARY 1963

PRODUCTION ENGINEERING MEASURE FOR THE IMPROVEMENT OF GERMANIUM ALLOY POWER TRANSISTORS

CONTRACT NO. DA-36-039-SC-86724

Placed by:
U. S. Army
ELECTRONICS MATERIEL AGENCY
Philadelphia
Pennslyvania

Contractor:

CLEVITE TRANSISTOR
A Division of Clevite Corporation
200 Smith Street
Waltham 54
Massachusetts

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PRODUCTION ENGINEERING MEASURE FOR THE IMPROVEMENT OF GERMANIUM ALLOY POWER TRANSISTORS

THIRD QUARTERLY REPORT

31 October 1962 - 31 January 1963

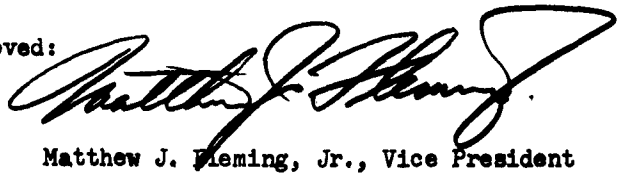
Object:

Establish the capability to manufacture Germanium Alloy Transistors Types 2N297A, 2N1011 or 2N1120 with a maximum operating failure rate of 0.05% per 1,000 hours at a 90% confidence level as an objective.

SIGNAL CORPS CONTRACT NO. DA-36-039-SC-86724

Report prepared by George Wallis, Manager of New Products Development Department of Clevite Transistor, a Division of Clevite Corporation.

Approved:



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31 OCTOBER 1962 - 31 JANUARY 1963

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Placed by:

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I ABSTRACT

1 Life test results on jet rinsed transistors are discussed.

2 Initial and life test results are presented for transistors on which surface passivation by oxidation was attempted.

3 Our welding procedure was investigated and it was determined that erratic results were obtained due to insufficient control over the dessicant which is dispensed during this operation. Steps have been taken to correct this situation.

4 Work on the failure analysis of units as received from production is described.

5 Experimentation on surface passivation by organic coats have been continued and life test results are given. Changes in the electrical parameter are reported for coated and non-coated unwelded transistors during a humidity cycle.

6 A new method has been proved out for introducing helium into the welded transistor for purposes of leak detection. Funds for a helium leak detector have been approved and an order has been placed. Work on associated equipment is in progress.

7 In the course of work on the activation of our present dessicant, $CaSO_4$, it was found that molecular sieve pellets give superior results, particularly during high temperature storage.

8 Work has started on the redesign of the internal clip and data are presented.

9 Results are given for approximately 1,000 transistors with ten mil thick collectors versus about 750 transistors with our standard five mil collector.

10 Prototype jigs have been designed and built which will reduce by a factor of three the number of times an unwelded transistor is handled from final surface treatment to welding.

11 A homogeneous lot of 3,000 transistors was manufactured and put on 90°, 125°, and 145°C storage test, elevated temperature cut-off test and step-stress test. Results are presented and failure modes are discussed.

II PURPOSE

Production Engineering Measure (PEM) for improvement of production techniques to increase the reliability for the transistors designated below.

This shall include all work necessary to establish capability to manufacture the specified transistors utilizing the improved production techniques including all quantities of samples to be delivered, actual modification of production equipment to incorporate the improved technique, performance of the necessary tests to demonstrate the capability of the improved production line and the preparation and distribution of reports. The above work shall be performed for the following item:

Germanium Alloy Transistor types 2N297A, 2N1011 or 2N1120 with a maximum operating failure rate of 0.05% per 1,000 hours at a 90% confidence level at 95°C as an objective. The failure rate is an objective and as a minimum all process improvements specified below will be performed toward attaining or exceeding the specified failure rate.

PROCESSES TO BE IMPROVED

a. Cleaning Procedure

b. Surface Passivation by Oxidation

c. Surface Passivation by Organic Coats

d. Activation of Desiccant

e. Redesign of Internal Clip

f. Redesign of Collector Pellet

g. Handling in Production of Transistor Sub-Assemblies and Piece Parts

h. Hermeticity

In accordance with the letter by the Contracting Officer, dated 5 February 1963, items d. to g. above replace the following two processes

specified in the original subject contract:

1. Novel Method of Alloying
2. Increase in Emitter Efficiency

Also in accordance with the letter the proposed process improvement, "Punch-through Limited Transistors" was not added to the processes specified in the contract.

III-1 CLEANING PROCEDURE AND SURFACE PASSIVATION BY OXIDATION

Most experiments were performed in matrix form with various rinsing treatments and bakes as the factors. In the presentation of the results it will therefore be necessary to combine the same data in several different ways. Where it seemed desireable, data from two or more nominally identical experiments have been combined. Most of the experiments in this section were placed on 145°C storage for relatively rapid evaluation of reliability. For a correlation of 145°C storage with storage at 125°C and 95°C see Section III-8.

In general, treatments were evaluated on the basis of Icbo and Iebo, both measured at 60 volts. Ib has contributed to failures only in a very minor fashion, and hence it has usually been omitted from the presentation of results.

In the course of the surface work the soundness of the following process was questioned: after final surface treatment the clip connecting the emitter and base ring to the terminals is fused electrically so as to open-circuit the shorted emitter-base connection. It was suspected that metal vapor generated during the fusing might deposit on the germanium and affect the reliability of the transistor. Experiment 13 was, in part, designed to point out any difference between units with fused clips and units which had the clips cut. As can be seen from the frequency distributions, Exhibit 1, of Icbo at 0, 72 and 168 hours of storage at 145°C no significant difference was found. Hence, in the experiments to be described, the clips were usually fused. However, as a precaution the experimental units had the clips fused before rather than after etching. This procedure also made it possible to eliminate from the experiments any transistors with high emitter-base floating potential.

The following rinsing procedures were employed:

1) Jet rinsing of individual units with ultra-pure water from a Barnstead unit as described in the second quarterly report. The temperature of the water varied from 60 to 210°F.

2) The above rinsing procedure followed by drying with a nitrogen gun.

Following rinsing units were given the following bakes in randomized experiments:

1) Dry oxygen baking from 50 to 150°C.

2) Dry nitrogen baking from 100 to 150°C.

3) Oxygen and steam baking from 100 to 150°C.

4) Nitrogen and steam baking from 100 to 150°C.

A) Results - Jet Rinsing

In the second quarterly report is was stated that jet rinsing had no effect on the initial distributions of Icbo, Iebo and Ib. This was further confirmed during the early part of the third quarter. As will be seen below the same is true for performance during high temperature storage.

Exhibit 2-A shows frequency distributions of Icbo and Iebo at 60 volts at 0, 168 and 333 hours storage life (145°C) for units which were rinsed until the resistivity of the outlet water approached that of the inlet rinsing water. Exhibit 2-B shows corresponding results for units which have been given a final 10 second rinse. The two sets of distributions are very similar and we conclude that no difference exists.

Exhibit 3 makes a comparison on the same basis as the above between units which were given a hot water rinse in the region of 180 to 190°F and the units which were rinsed in the region of 70°F.

Again the conclusion is that no difference exists between the hot and cold rinse.

Exhibit 4 compares the Icbo at 60 volts of hot rinsed units and control production units at 0, 168 and 333 hours of storage at 145°C. The conclusion once more is that rinsing has no effect on units.

All the above evidence is typical of what has been found in regard to the effect of rinsing on reliability. Of course, it is always possible that the beneficial effects of a treatment are masked by extraneous effects. Thus it might be advisable to have another look at jet-rinsing at a later stage. For the time being, however, no further work on jet-rinsing is planned.

B) Results - Surface Passivation by Oxidation

In summary, bakes at around 100°C in a dry oxygen atmosphere gave the best results initially and after high temperature storage. Bakes at the same temperature in dry nitrogen were only slightly inferior. Bakes in wet atmospheres invariably gave significantly poorer results.

Since our baking procedure in dry nitrogen, though in principle quite similar to our production procedure, nevertheless gave better results than the latter, the suspicion arose that some of the production equipment is contaminated. This is being followed up.

Exhibit 5 shows the effect of 145°C storage on the Icbo distributions of three groups: a control group, a group that was baked at 150°C in dry oxygen and a group that was baked at 150°C in dry nitrogen. No significant differences between the groups are

apparent at 168 and 333 hours of storage.

In Exhibits 6 and 7 similar data are shown for bakes in dry oxygen and nitrogen at 100°C. Exhibit 6-A presents the zero hour distributions of Icbo for the three groups. A somewhat tighter distribution is apparent for the oxygen group than for the nitrogen and control groups. Exhibit 6-B shows the same groups after 333 hours of storage at 145°C.

Evidently, the control group has a broader distribution than the other groups. Note that the only failure (Icbo > 6 ma at 60 volts) in the oxygen-baked group is an open due to a faulty solder contact between the base ring and clip. The statistically significant high incidence of failure in the nitrogen-baked group is puzzling since the distributions for oxygen and nitrogen baking are equally tight. Both have a "normal" appearance even though an obvious shift has taken place.

Much the same conclusions may be drawn from the Iebo distributions for the above groups (see Exhibits 7-A and 7-B). The effect of oxygen baking at 100°C is to retain better than zero hour distribution, the first interval being the most heavily populated. The effect of nitrogen baking at 100°C is not as marked but still decidedly better than the control, the first and second intervals being equally populated.

These results gain in significance in that they represent data from three different experiments.

In Exhibits 8 and 9 we compare the effect of 100°C bakes in dry and wet oxygen. Here, wet oxygen denotes oxygen bubbled through

hyper-pure water at 70°C. Exhibit 8-A shows the zero hour distributions for Icbo at 60 volts. The group baked in wet oxygen has strikingly higher leakage currents than the group baked in dry oxygen. The corresponding distributions after 333 hours at 145°C storage are shown in Exhibit 8-B. The distributions of the two groups are more nearly similar than at zero hours but the wet oxygen-baked group has a longer tail resulting in failures where there are none in the dry oxygen-baked group. The corresponding distributions for Iebo at 60 volts are shown in Exhibits 9. The zero hour distributions for the two groups are quite similar (see Exhibit 9-A). However, after 333 hours at 145°C storage the wet oxygen-baked group has higher leakage than the dry oxygen-baked group. The two distributions have similar tails. (Exhibit 9-B)

Further experiments along these lines have been made and put on high temperature storage. Provided the above results can be reproduced, a 100°C bake in dry oxygen will be recommended to production.

C) Investigation of Welding Operation

From the results reported so far it was fairly evident that the effects of bakes under the above conditions were partially masked by other poorly controlled factors. Some positive steps towards tighter control have been taken. For instance, when transistors have to be moved from one location to another, they are transported in a dry box on wheels through which a continuous flow of nitrogen is maintained. Again, a start has been made at baking caps at 200°C prior to welding.

One source of variability is the welding process. A homogeneous lot of transistors was divided into groups of 30-35 units which were welded consecutively. Exhibit 10 shows the percentage of units within each group which had an initial Icbo at 60 volts $>$ 1 ma. With time, the fluctuations become smaller and the percentage of high leakage units decreases.

Sealing results with respect to Icbo are shown in Exhibit 11 for 333 hours storage at 145°C. Here, Seal 1 denotes the first set of units which were welded after the machine had been standing idle. Seal 2 denotes units which are similar to those in Seal 1, except that they were welded subsequent to the first group. One can see that there is a considerable difference in the number of defectives. Calculation shows that there is a 95% probability that this difference is significant. Exhibits 12-A and 12-B show similar data except that the transistors denoted by Seal 1 were welded on a machine which had been in continuous operation for some time. No differences between Seal 1 and Seal 2 are apparent. The relatively large number of failures is probably due to the fact that during storage the oven accidentally ran up to 160°C for a period of unknown length.

The differences between the groups may have been due to 1) variations in ambient during welding, 2) differences in the operation of the welder itself and 3) variations in the moisture control of the dessicant, $CaSO_4$, which is automatically dispensed during welding. In view of the fact that differences in the reliability of subgroups occured between groups which were welded consecutively, it was concluded that the ambient atmosphere is

not a major factor. An examination of units in different groups failed to show up differences in weld quality. Failures were helium leak tested and proved to have as low leak rates as good units. We therefore feel quite certain that much of the variability from group to group must be assigned to the dessicant. This will be discussed in detail in a later section.

D) Failure Analysis of Production Rejects

This work is largely a continuation of the effort which was started during the second quarter. It was realized that high emitter-base floating potential arises from a non-uniform current flow from the base into the collector. The effect is large if the current density is high and confined to a small area, preferably underneath the emitter. This does not necessarily mean that the total current flowing into the collector is particularly large. Non-uniform current flow can, of course, be due to many causes such as flaws in collector alloying, non-wetted regions, small areas which break down prematurely and cracks on the dice. Only under extreme conditions can the surface lead to a high floating potential.

In order to establish how severe a problem cracking of dice was 43 units having an emitter-base floating potential $\geq$ 0.5 v at 60 volts were dismantled and etched under a microscope. Of the total (which represents about 40% of all units in this particular lot) 18 units, i.e., 42% had cracks. These cracks appeared during the etching procedure. Many originated on the emitter side of the die under the base ring area. In most cases these cracks became visible on the emitter side some time before appearing on

the collector side. The reason for high floating potential in the remaining transistors has not been established though it seems likely to be due to poor collector alloying. These floating potential rejects originate, as previously reported, mainly during the soldering of the alloyed assembly to the header. Some units also fail during etching and a few during welding and subsequent burn-in. The percentage of these latter failures seems to bear a proportionality relationship to the percentage already having failed. This suggests that these subsequent failures were potential failures due to stresses set up during the alloying and/or soldering operation. One of the hypothesis being investigated is that there is a thermal mismatch between the Nickel-Iron base ring and the germanium die. The thermal properties of molybdenum are less critical and approach those of germanium more closely. Units using this material as base rings have been made up together with a control group. Initial results indicate that fewer rejects are generated by the molybdenum base rings.

As is to be expected there is a pronounced correlation between floating potential and collector leakage. In an experiment alloyed dice were selected which had a floating potential $(Veb)_f < 0.5$ at 80 volts. The dice were then processed and remeasured for $(Veb)_f$ and Ico with the following results.

$(Veb)_f$ @ 80Vbc in volts	Total Number of Units	Number with Ico > 1ma. @ 80V	% > 1ma
< 0.1	19	3	15.8
0.1	117	18	15.4
0.2	22	5	22.7
0.3	9	6	66.7
0.4	5	5	100.
> 0.5	12	11	91.7

The results are interpreted as follows. About 15 to 20% of the transistors have a relatively high surface leakage on account of surface conditions. High leakage in the remaining units is due to bulk defects in the collector which may affect the reliability of the units. Interestingly enough, 33% of the units with $(Veb)_f$ = .3 volts and 8% of the units with $(Veb)_f \geq .5$ volts have relatively low leakage. Nevertheless, these units are of questionable reliability.

That high collector leakage in transistors with normal floating potential is due primarily to surface conditions was confirmed in the following experiment.

Units with an Ico > 1ma at 60 volts and having a floating potential $(Veb)_f$ < .3v at 80 volts were uncapped and etched electrolytically for an extra half minute. Distributions of Icbo and Iebo before and after the additional etch are shown in Exhibit 13. The etch brought about a dramatic improvement in collector leakage but not in emitter leakage. This suggests that under present conditions the etching of the emitter is optimized but that the collector is insufficiently etched. For

confirmation, the following randomized experiment was performed.

Control units (etched for 1½ minutes) were run versus units which had been given a regular etch and drying followed by an extra ½ minute etch, rinsing and drying. There was a noticeable difference between the two groups; the doubly etched units showing a much tighter spread in Icbo at 60 volts (See Exhibit 14).

Thus there is much evidence that under present conditions the collector could sometimes benefit by a longer etch. This is not unexpected in view of the following. 1) Due to the geometry, the hole flow pattern is such as to promote a higher etching rate around the emitter than around the collector. This effect is seen clearly in sections of etched transistors. 2) During soldering, a film of indium is sometimes smeared over the collector junction. The film can only be removed by extensive etching. 3) Frequently, the soldered die fails to sit squarely on the pedestal. In such cases non-uniform etching of the collector junction is to be expected.

Although less germanium is etched away around the collector than around the emitter, it is more than adequate where conditions 2) and 3) are not present. This was demonstrated in experiments with reduced etch times. Two approaches are being taken towards the elimination of 2) and 3). First, work with a redesigned clip, to be described in a later section, promises to improve alignment and reduce tipping. Second, a slight reduction in the diameter of the pedestal is being planned.

It is expected that the above improvements will permit a reduction in etch time without sacrificing low leakage. This would be highly desireable because it would result in a lower value of Veb.

In the course of the experiments with etching conditions it was also investigated whether step etching is more effective than continuous etching. Etches of 1 minute and $\frac{1}{2}$ minute followed by another etch of $\frac{1}{2}$ minute were tried. The latter etch proved inferior whereas the former etch (1 + $\frac{1}{2}$ minute) was about equivalent to the control. Thus, nothing is to be gained from step etching.

III-2 SURFACE PASSIVATION BY ORGANIC COATS

A) Silane Coatings - Life Test Results

Transistors, silane coated as indicated in the second quarterly report, were subjected to 145°C storage life tests. On early lots silane coatings (a) changed the normal slow deterioration in gain to a slow improvement, (b) showed no significant change in Icbo or Iebo degradation or failure rate.

Because of the evident improvement in gain and the low confidence level of the changes in reverse characteristics, larger quantities were coated and subjected to storage test at 145°C. Exhibits 15 through 18 show a composite summary of the frequency distributions of Icbo and Iebo of all coated units versus the uncoated units, the latter having been normalized to make their total equal to the number of coated units. No significant effect of coating is discernible.

Results using the contract failure criteria are summarized in the following tables.

100 Hours @ 145°C Storage Life Test

	# Units	# Failures Icbo	# Failures Iebo	% Failures Icbo	% Failures Iebo
Coated	364	4	1	1.1	0.27
No Coat	162	3	0	1.8	0

252 or 344 Hours @ 145°C Storage Life Test

	# Units	# Failures Icbo	# Failures Iebo	% Failures Icbo	% Failures Iebo
Coated	118	4	1	3.4	0.85
No Coat	58	5	1	8.6	1.7

Improvement of significant magnitude due to coating is doubtful. In particular, the consistency between the 100 and 252 hour tables does not give weight to significance since many individual failures are in both groups.

The most striking, and puzzling, aspect of life tests on coated units is the beneficial effect on gain, in spite of it being no help to junction reverse characteristics. See, for instance, Exhibit 19. The superiority of coated units against gain degradation is fairly clear and consistent. Unfortunately, in terms of contract specification it is not important, that is, gain is rarely a source of failure. No gain failures were observed that were not simultaneous with collector failure.

Several hundred additional units have been coated and as completed, their life test data will be added to these.

In addition, some of the coated units will be tested at 125°C instead of 145°C. The intent here is to strengthen the applicability of the conclusions from the high temperature (145°C) to the 95°C contract objective.

Little more of this coating will be done, subject of course to reconsideration if the above conclusions change.

B) Silicate Coating - Life Test Results

During the second quarter some transistors were given an

alternate coating derived from ethly silicate. As an example, life tests on lot F 1-20 are shown in Exhibits 20, 21 and 22. As compared to uncoated controls, no significant effect on reverse characteristics is found for these coatings. Effect on gain is slight if significant and in any case less than on silane coatings. No future work is planned on ethyl silicate coatings.

C) Silane Coating - Vacuum Procedure

In addition to the flushing type silane procedure discussed, silane coating can be applied at reduced pressure within a vacuum system. Here the higher diffusion rates at low pressures offer a potential advantage in uniformity and coverage. Regions with limited access such as the edge of the collector junction might profit from its use. Though much less convenient from a production standpoint, it seemed desirable to see whether or not its coatings would provide superior reliability.

Briefly its operation consists of the following steps:

1) Evacuation of the system.
2) Distillation of chloro-trimethyl silane to a measuring chamber, adjusting its volume to 2 units by pumping off the excess, and vacuum distillation transfer to a sample reservoir.
3) Repeating (2) above for 9 units of di-and trichloro silane.
4) Evacuation and subsequent back filling to a desired water partial pressure, of the reaction chamber with the transistors.

5) Addition of the silane mixture to the reaction chamber.

6) After the reaction period, evacuation, then air filling and opening of the reaction chamber.

7) Air bake of the units for 2 hours at 125°C.

8) Covering of the transistors with acetone, boiling three minutes, and decanting.

9) Repeat of (8) above for a total of three times.

10) The units are then baked in air for two hours at 125°C and capped.

A few lots of transistors have been coated and if their life test results look promising, this work can be expanded.

D) Electrical Testing of Uncapped Units at High Relative Humidity

With a view towards evaluating the permeability of silane coatings, open units were tested electrically under high humidity conditions. Icbo and Iebo were chosen as the parameters most sensitive and watched for changes from the dry to the humid state. In order to establish equilibrium, exposure lasted at least two hours and often overnight.

The humid atmosphere was generated by mixing water saturated and dry nitrogen and argon, the relative humidity being controlled by the relative proportions. With the transistors in racks in a plastic bag with glove inserts in which a transistor test socket was mounted, it was possible to store and test units without exposure to other than the controlled atmosphere.

Early in the testing it was apparent that from dry to 30 or 50% relative humidity, large variations between units were present. Some junctions showed no change while others increased

by more than an order of magnitude. In general these changes were small for silane coated units in comparison to uncoated controls. Typically in Lot T at 50% relative humidity the mean Icbo for coated units was .09 ma versus 4. ma for uncoated units. As this testing progressed it soon became apparent that not all uncoated junctions were affected by a selected high humidity. For example, in Lot T referred to above, the emitters of the uncoated reference units showed little change at 50% relative humidity. The Iebo mean increased from .04 dry to only .05 ma humid.

Less drastic but variable effects of dry versus humid tests are shown in Exhibit 23. With dry versus 30% relative humidity values of Icbo plotted on log-log graph paper, units showing no change fell on the 45 degree line. Units with high Icbo's due to humidity fall to the right of the line. Here, the coated units show relatively little change, probably a slight improvement in the high relative humidity state. Uncoated units show far more scatter, the extreme changing more than an order of magnitude.

The variable effect of humidity is probably due to the residual state of the surface where the junction emerges, its contamination, oxide form, etc. If these same factors are, in part, responsible for life test failure and degradation, then humidity testing and sorting might result in improved reliability. This hypothesis is observed to be consistent, at present, with the fact that our emitter junctions generally deteriorate less than the collector junctions.

Several hundred units have been tested at high humidity. Correlation or lack thereof after completion of their life tests should establish the usefulness of this technique.

E) Failure Analysis

On checking over a group of failed units accumulating for failure analysis, it was noticed that Icbo and Iebo values had decreased considerably since the completion of the 145°C storage life test. Exhibit 24 shows the results of 30 day room temperature recovery. All units show significant recovery, averaging a reduction by 50% in reverse current. It is interesting that this applies equally to the good emitters as to the failing collectors on these same units. This adds support to the hypothesis that some of the "bad" units are being affected by the same mechanism as "good" units.

These same 16 units were opened to atmosphere and measured after one and also after twenty-four hours. No change was noticed except for one unit which showed a dramatic Icbo drop, from 5.0 to .5 ma.

In the quest for a better understanding of the failure mechanism it seemed desirable to try to determine whether:

1) Failures are units in the tail of the normal distribution of all the units or,
2) Whether failures are the result of an occasional chance occurrence having no bearing on the general degradation of the bulk of the units.

One of the simplest ways of indicating this is to plot the data on a graph with a probability scale. Here the cumulative

normal distribution yields a straight line, the deviation from which is relatively easy to recognize. Lot L of silane coated units are shown before and after a 100 hour storage life test at 145°C in Exhibit 25. Here the distributions are suprisingly normal. Well within a factor of two, the number of failures are anticipated at any specification level, from the behavior of the bulk of the units.

This result was also confirmed on a larger lot of 300 uncoated units. This means that a significant part of the failures are due to a mechanism operating on most of the units. It does not, however, rule out the possibility that part, perhaps up to half of the failures at our specifications, are due to an occasional mechanism affecting only a few units. These points are discussed further in Section III-8.

III-3 HERMETICITY

A new method of leak detection has been evaluated. The method consists of saturating the dessicant ($CaSO_4$ powder) with helium, introducing the dessicant into the unit prior to welding and testing of the welded units on a Veeco mass spectrometer prior to any further operations. Presence of helium in the units was verified by drilling holes in the caps of non-reading units and re-testing with resultant off-scale readings. Some drilled units were tested daily to determine if a large leak could lose so much of the helium that a catastrophic leak could pass the test due to a time lapse between welding and testing. After one week these units still produced high readings, thus demonstrating that time lapse is not important to this method.

The trial consisted of introducing the helium into the dessicant simply by a regulated flow from a tank of helium into the heated dessicant container at the welder, allowing a period for initial saturation, then sampling the production. It was found that a flow of 5 cfh for 2 hours would sufficiently activate the dessicant to produce good results, and then the flow could be reduced to 2 cfh.

Leak testing of welded assemblies has been done on a sampling basis to prove out the above method of leak detection.

The main advantages to this method are the rapidity of testing, since it eliminates the normal four hour pressurizing procedure; the ability to detect smaller leaks, since more helium is in the unit with a smaller leak than can be introduced by pressurizing, and the freedom of the unit from helium trapped in exterior crevices which would cause small indications which could be read as small leaks.

The method will be a part of the process, with helium piped from a central supply through refrigerated drying columns to the dessicant dispenser on the welder, and a mass spectrometer adjacent to the welder to be used in continuous sampling of the product, both for control of the weld process and assurance of a small probability of escape of leaking units. A manifold capable of testing 24 units simultaneously is being fabricated, and a mass spectrometer is on order.

As will be described in the next section, there is a possibility that molecular sieve will be substituted for the calcium sulphate dessicant now in use. Hence, an experiment was made to determine if this method is applicable to the sieve. The molecular sieve pellets were activated for one hour at 400°C in a helium atmosphere, removed and after a time lapse of approximately 15 minutes were inserted and welded into units which were tested in the mass spectrometer. No leaks were found and presence of the helium in the unit was verified by twisting a terminal to break the seal, whereupon off-scale readings were obtained.

When this method is installed all of our subsequent handling procedures will be scrutinized to eliminate any practices which could cause excessive stress to the glass-to-metal seals, which are the weakest part of the unit and the most probable area for damage.

The tentative plan for sampling calls for continuous sampling of batches of 24 units, which will allow testing of 1/3 of production while the welder is operating. The non-operating time will be utilised in screening production lots which gave evidence of leaks. Corrective action will be initiated upon finding a single leak in a sample.

Pending introduction of this method as a documented procedure, daily sampling will be performed to establish the normal occurrence of defective welds.

III-4 ACTIVATION OF DESSICANTS

As described earlier, the majority of life test failures during the last few months have been diode failures. Furthermore, failure analysis indicated that most of the diode failures were due to deterioration of the surface. After consultation with the Signal Corps, it was therefore decided to investigate the effect of dessicants.

Since then, further evidence has come to light which strongly suggested erratic behavior of our dessicant, i.e., $CaSO_4$ powder. In Section III-1 we described a comparison of two groups of transistors from a homogeneous lot: group 1 was welded on a machine that had been standing idle while group 2 was welded on the same machine immediately following group 1. Frequency distributions were far broader for group 1 than group 2 and life test data also favored the latter group. The following explanation fits the facts. When the welding machine is idle room air backs into the dessicant dispenser, and powder near the bottom outlet absorbs moisture even though dry nitrogen is passed into the top of the dispenser at all times.

The above was an extreme case. During further work it became evident that the $CaSO_4$ produced erratic effects not only as far as the first units after welding start-up were concerned but also in continuous operation.

While investigating possible reasons for this, it was found that the dispenser was heated insufficiently so that the dessicant was not maintained at a minimum temperature of 125°C as specified. In order to correct this situation new heaters have been installed in the dispenser. It remains to be seen whether this will lead to greater uniformity of the product.

During work on the optimum activation temperature for $CaSO_4$ we also

looked into the possibility of using other dessicants and found that molecular sieve gave improved results as far as initial electrical parameters were concerned.

Consider, for instance, one of the early experiments comparing $CaSO_4$ with molecular sieve powder and molecular sieve pellets. The $CaSO_4$ was activated 48 hours at 170°C, and the molecular sieve powder and pellets were activated at 300°C for 8 hours. One hundred units were chosen at random from the production line. These units were divided into three groups and capped with calcium sulphate, molecular sieve podwer and molecular sieve pellets.

The distributions of Icbo at 60 volts, Ib at Ic = 10 a and Ib at Ic = .5 a are shown in Exhibit 26 for the dessicants $CaSO_4$ and molecular sieve pellets. Distributions for the molecular sieve powder are not shown because the powder gave only marginally better results than the $CaSO_4$. Units containing molecular sieve pellets however, are considerably better on Ico at 60 volts, slightly better on high current gain, and about equal in low current gain.

On the basis of such results a group of experimental units were fabricated for life testing. These consisted of 35 $CaSO_4$ filled units and 35 units containing molecular sieve pellets. Initial average lot values showed Icbo and Iebo of the molecular sieve group was slightly lower than the control group. The molecular sieve average Ib however was slightly higher than the controls. This showed that the molecular sieve produced a humidity within the package that was less than optimum for Ib but closer to optimum for Icbo and Iebo.

A storage test was run at 145°C for a total of 333 hours. Exhibit 27-A shows average lot values at 0, 48, 168 and 333 hours for Icbo and Iebo. The corresponding values for Ib at Ic = 2 a are shown in Exhibit 27-B.

The change in all molecular sieve parameters is less than 40% that of the control group. The control group produced four Ico failures and one Ib failure out of 32 total units while the molecular sieve produced no failures. Distributions of Icbo for $CaSO_4$ and molecular sieve pellets are plotted in Exhibit 28.

Although the failure rate in the control group was untypically high, the units in the molecular sieve and control groups were picked at random from the same manufacturing lot so the difference must be attributed to to the molecular sieve at this time. This experiment has been continued on life test for measurement at 667 and 1,000 hours.

Beacuse of the initial success with the molecular sieve pellets it was decided to run additional larger experiments. The pellets were activated at 310°C in a constant flow of dry nitrogen. During transfer to production they were stored in a nitrogen box which had a continuous flow of gas. Thus, the pellet was in contact with room air only during transfer from the furnace to the dry box and from the box to the welding head. Units made with these pellets look promising and are at present on storage life.

III-5 REDESIGN OF INTERNAL CLIP

The major problem with the present clip is that the emitter tab fails to penetrate into the emitter about 80% of the time, thus preventing the body of the clip from resting against the base ring of the unit. As a result there is poor soldering or a lack of soldering between clip and base ring, and additional hand soldering becomes necessary. Soldering outside the hydrogen atmosphere of the furnace requires flux which can spread on the unit and base. This flux is removed in a trichlorethylene bath. However, it is doubtful if all flux is removed in all cases with the remaining flux being a detriment to reliability.

A second difficulty with the present clip is that the three tabs which are bent about 90° to the clip body sometimes rest on top of the clip after soldering. This prevents proper setting down and soldering and also allows the die to be tipped and misaligned on the dimple. A misalignment can place part of the collector junction in a position with respect to the dimple that prevents proper etching and rinsing. It can also cause some indium to run across the junction.

The clip was redesigned as shown in Exhibit 29. A fourth tab is added and all the tabs are lengthened so as to provide good centering of the die before and during soldering.

It can also be seen that the redesign provides for a decrease in the cross-sectional area of the clip at the points where fusing takes place. This substantially reduces the current required for fusion and, hence, the amount of vaporized brass or tin.

Two lots of the new clips were run with the result that they settled into the emitter and against the base ring with a greater frequency than the present clips. The conclusion was that either the slightly heavier

weight of the clip pressing down on the emitter tab or the amount of tinning on the clip aided in wetting and settling, or both.

To investigate the amount and consistency of tinning, a number of clips from various lots were sectioned and microphotographed. These sections showed large variation in the thickness of the plated tin coat between each side of the same clip, between clips, and between lots of clips.

Incoming inspection procedure has been modified to insure sufficient tinning on accepted lots. Also two special lots of tin clad brass clips have been ordered to determine the difference, if any, between tin clad and tin plated clips.

As indicated above, the greater weight of the new clip appeared to improve the quality of the solder joints. Further efforts at improvement were made along two avenues.

First, a jig was made to bend the tip of the present emitter tab 90° so it enters the indium edge first. Also a lot of modified clips were ordered according to this design as shown in Exhibit 30. The idea was that by decreasing the initial contact area between the tab and the molten indium the former would sink into the indium more readily and thus permit settling of the clip assembly. In addition, this should also improve the wetting of the emitter tab

In the second approach, weights were employed during soldering. One hundred small graphite weights $\frac{23}{32}$ dia. by $\frac{3}{32}$ thick were made. Several lots of clips including present clips, newly designed clips, and 90° emitter tab modifications of both, were run with these weights. Results in a run incorporating the various approaches are shown in the following table.

Soldering	# of Transistors Without Gap Between Base Ring and Clip
1) Present clip	6/50
2) Present clip with modified emitter tab	15/50
3) New clip	44/50
4) New clip with modified emitter tab	24/25 20/25
5) New clip with weights (carbon disk resting on emitter tab hump)	80/80
6) Present clip with weights	45/50

The results can be summarized as follows. Setting of the clips is greatly assisted by weights. The new clip design is a substantial improvement over the presently used design. The merit of the 90° modification is clearly established for the present clip but is in doubt for the new clip.

III-6 REDESIGN OF COLLECTOR PELLET

At the time the transistor was designed it was decided to make the collector pellet as thin as possible in order to reduce the thermal resistance. Thus, present collector pellets are 5 mils thin and upon alloying produce a recrystallized region of about 1 mil thickness. Under optimum alloying conditions, the design works satisfactory. However, in practice one finds that alloying conditions frequently prevail on the manufacturing line so that the 16 mil thick emitter pellet alloys well whereas the 5 mil collector pellet alloys quite poorly. Typically, there is an abundance of small regions where no recrystallized region is apparent. Hundreds of sections support this statement. The difference in the quality of alloying is clearly attributable to the thickness of the respective indium pellets. Unavoidably, some regions of germanium are wetted by indium at a somewhat lower temperature than are others. Where there is enough indium backing this is of no great concern because as the alloying temperature is raised there is sufficient indium available to wet the remaining regions and small differences in the thickness of the recrystallized regions tend to be eliminated. However, where only a small thickness of indium is present, the germanium region which wet first will dissolve all available indium and germanium regions which potentially could be wetted at a higher temperature will remain unwetted because of a lack of indium.

A non-uniform collector region produces non-uniform current flow which compromises the reliability of a transistor under operating conditions. For a given level of total current the defective regions in the collector carry abnormally high current densities and develop hot spots which may

lead to burn-out. For a given reverse voltage, the defective collector regions generate higher currents or in some cases break down prematurely. Hence, reverse characteristics are soft and the emitter-base floating potential is high.

For all of the above reasons, a number of experiments were run comparing 5 mil and 10 mil thick collectors. As expected, the quality of alloying was much improved in that a substantial reduction in unwetted regions was found. Electrically, most of the emphasis was put on the measurements of BVces because it is a sensitive measure of the occurrence of hot spots as indicated by burn-out or "ballooning". The results are tabulated below. Only those transistors are included which had BVces $>$ 50 volts. The number of such transistors in each experiment and the percent of units which burned out or ballooned at a collector current Ic $\leq$ .8 a are shown.

	5 mil Collector		10 mil Collector	
Experiment	# Units	% Ballooners	# Units	% Ballooners
69	30	83	67	40
70	72	61	77	32
71	74	64	73	44
73	--	--	107	35
75	60	53	135	36
76	23	61	51	69

A similar breakdown follows for units ballooning at Ic $\leq$ .5 a.

Experiment	5 mil Collector # Units	5 mil Collector % Ballooners	10 mil Collector # Units	10 mil Collector % Ballooners
69	30	44	67	18
70	72	33	77	18
71	74	39	73	32
73	--	--	107	14
75	60	42	135	25
76	23	48	51	21
Pilot Run	500	14.6	500	11.2

Totalling all experiments, but excluding the pilot run, we had 162 ballooners or burn-outs (63%) at Ic $\leq$ .8 a and 104 (40%) at Ic $\leq$ .5 a in a total of 259 transistors with 5 mil collectors. This compares with 215 ballooners or burn-outs (37%) at Ic $\leq$ .8 a and 120 (21%) at Ic $\leq$ .5 a in a total of 582 transistors with 10 mil collectors.

Dice from the same material were used in experiment 76 and the pilot run. Thus, the material had no bearing on the large percentage of ballooners in the former and the small percentage of ballooners in the latter. The differences can be accounted for by the quality of alloying.

Data on Icbo are far less complete and also harder to interpret since it is affected by many factors such as etching, final surface treatment, condition of drying oven and dessicants. Distributions of floating potential favor the 10 mil collector.

Six more pilot runs of 500 transistors each are planned, one of which has been started. After results have been analyzed a decision will be made whether 10 mil collectors are to be introduced into the line.

III-7 HANDLING IN PRODUCTION OF TRANSISTOR SUB ASSEMBLIES AND PIECE PARTS

The reliability of transistors unavoidably is affected by the amount of handling and the care expended in handling. This is true for welded transistors: units are dropped and jarred with a resultant possibility that dice crack; during insertion into test equipment, leads are bent and may crack the glass-to-metal seals. The same is true to a far greater extent for the transistor before it is welded where careless handling will result in the introduction of contaminants. In the absence of mechanization proper jigging must therefore be designed which will reduce the amount of handling to a minimum.

The most critical period of handling is between the final surface treatment and encapsulation. At present the units are removed from the final rinse on bars which carry 10 units. The devices are removed from the bars and placed on wire mesh trays which are run through a drying furnace. The units are then removed from the tray by an operator one at a time, placed in a fixture for fusing clips, and then replaced by the operator. At the testing stations the units are again removed from the trays, tested and replaced. Finally, during cap welding an operator picks up each unit and places it on the welder.

After final surface treatment, each unit is thus handled a total of six times by four different operators.

Although as much care as possible is taken during these handling operations, there is always the chance that some contaminants will come in contact with the units.

In order to reduce the amount of handling and make it less susceptible to contamination a scheme was worked out by which the units can be placed

on a carrying rack and tested and fused on the same rack. A special jig has been designed and built for blowing the clips while they remain in the tray. This jig is shown in Exhibit 31. A similar jig, shown in Exhibit 32, was built to test the units without removal from their carrying tray.

With the new method, units are loaded onto the special trays as they are removed from the etch bars. They are dried, fused, stored and tested on these trays. The welder operator removes the units from the tray by the terminals and places them on the welder. The operation now has only two handling steps by two operators instead of the original six steps by four operators.

As an interim solution some of our present wire mesh trays have been teflon coated so as to make feasible the testing and clip fusing of units while being mounted in the tray. There are two drawbacks to this arrangement: 1) Units sit in the tray with the germanium facing up. Hence, dust can drop on parts which are to be later encapsulated. 2) During transfer, units have to be picked up by the ears. Since transfer is done by hand the danger exists that sometimes a critical part of the transistor is accidentally touched.

These objections are met by a newly designed aluminum tray. Here, transistors are mounted with the germanium facing down. Hence, transistors can be handled by their external leads.

Both systems of handling are at present being evaluated on the line.

III-8 COMPARISON OF LIFE TESTS AND ANALYSIS OF FAILURES

A homogeneous group of 3,000 transistors was assembled in production for the purpose of submitting the transistors to life tests, storage, step-stress and operating, under various stresses. It was hoped that these tests would throw some light on the occurrence of new failure modes as stresses are increased, and also that valid correlations could be established. In the following only those tests will be discussed in which a reasonable number of test hours have been accumulated, i.e., 350 units with 1,000 hours of storage at 95°C, 500 units with 1,000 hours of storage at 125°C, and 300 units with 336 hours of storage at 145°C. The results are presented graphically as distributions of Ico and Ieo, both measured at 60 volts, as a function of time (see Exhibits 33 (95°C), 34 (125°C) and 35 (145°C). Similar plots for Ib were omitted since virtually no failures occur in this parameter.

Before analyzing the data it should be kept in mind that all transistors received a 100 hour bake at 125°C prior to being put on life test. This bake is a normal part of our process.

A comparison of the 95°C and the 125°C distributions shows only a very slight difference. In both cases, there is a shift towards higher values of Ico and Ieo as the test progresses from 0 to 1,000 hours. Simultaneously there is a distinct broadening of the distributions. These trends are also evident from Exhibits 36 and 37 where the median Icbo and Iebo are plotted as a function of time for the three tests under discussion.

The broadening of the distributions is due almost entirely to a very gradual updrift of Icbo and Iebo values. At 95°C, the drift is sufficiently slow so that the tail of the distribution is well within the permissable

limits at 1,000 hours. At 125°C, on the other hand, the drift is somewhat faster and as a consequence the tail of the distribution at 1,000 hours comes dangerously close to the limit. Nevertheless, hardly any failures generated at this temperature during 1,000 hours are due to a gradual drift. Rather, the failed units characteristically are relatively stable for a long period of time and then rapidly drift out of specification. This is evident from Exhibit 38 where all failures, Icbo as well as Iebo, at 125°C are plotted as a function of time. Of the 6 failures only one is due to a slow drifter.

As the time on storage at 95°C or 125°C is extended beyond the 1,000 hours or alternately if the slow drifting process is accelerated by storage at higher temperature it should be expected that the tail of the distribution will eventually drift beyond the limits. This is seen to occur at 145°C storage (see Exhibit 35). From the distributions of Icbo and Iebo it is evident that the rate of drift is accelerated, and that the distribution broadens substantially over short periods of time. The median Icbo and Iebo increases rapidly (see Exhibits 36 and 37). Exhibit 39 which plots Icbo and Iebo of the defective transistors as a function of time shows that 5 out of 15 failures represent slow drifters.

Further evidence that a significant percentage of the failures are in the tail of the distribution is presented in Exhibit 40. Accumulative distributions of Icbo at 100 and 336 hours of 145 C storage are shown on log versus probability scales. The distributions are again normal, as previously found for Silane coated units. This demonstrates that a major failure mechanism is not just "occasional" but is operative in the degradation of the whole lot.

The question arises whether slow and fast drift is governed by the same mechanisms. As far as Icbo is concerned, we have established that both types of drift are purely surface phenomena. A very short etch, for instance, almost invariably reduces the leakage as shown in Exhibit 41. In this case, storage at 145°C resulted in a severe deterioration of the Icbo distribution. The transistors were opened and etched electrolytically for 30 seconds. This largely restored the original distribution.*

Nevertheless, there may be differences not only of degree but of a more fundamental nature. One might speculate that in the case of fast drift the die starts out relatively clean and becomes contaminated only after extended storage, the contamination originating from the package. The reason the collector junction is affected more frequently by this type of drift than is the emitter junction may be found in the fact that the former is less protected by $CaSO_4$ powder than the latter. In the case of slow drift, on the other hand, the contamination may, to varying

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* Severe deterioration during storage occured also in the Iebo distribution (Exhibit 41). Just as in the case of Icbo, re-etching brought about some improvement in Iebo. More striking, however, is the number of failures generated at this stage.

Unfortunately the units were damaged accidentally after re-etching and so it was not possible to analyze the failures. They may very well have been due to threads of indium which, having been undercut by the excess etching, extend across the junctions so as to effectively shunt it with a resistance, which could have a wide range of values depending on the geometry of the shunt. An effect of this type has been occasionally observed (Exhibits 42 and 43).

degrees, be present on the die from the start.

As far as Iebo is concerned the situation is different. Failure due to slow drift is less frequent. Re-etching of fast drifters as a rule fails to reduce leakage indicating that we are not concerned with a surface effect in the above sense. In some instances the source of trouble has been identified as a finger of indium bridging the junction. (See Exhibits 42 and 43.) In other instances a thin conducting film of undetermined material covers a part of the region between emitter and base ring which is quite etch-resistant.

At 145°C a failure mode appears which has not so far been observed at 95°C and 125°C, namely open emitters. The occurrence of open emitters during 145°C storage is not suprising. The indium emitter is soldered to a tin plated brass tab. If, during soldering, the concentration of tin in liquid indium exceeds about 5%, then the tin-indium alloy will remelt around 145°C. Jarring of transistors as they are taken out of the 145°C oven may therefore open up the bond between the emitter and the tab, particularly if wetting was poor to begin with. In the following, the open emitter failures will be disregarded since they represent a failure mechanism which is not active at 95°C.

At temperatures above 145°C, another failure mechanism was observed, i.e., cracking of dice. The units in question were a part of a group on step-stress tests. Temperature was the stress, the maximum temperature being 240°C. After the test all units with high floating potential were opened up, amalgamated and etched. Two of the 25 units had cracked dice. It is rather puzzling why dice which have been soldered at 400°C subsequently crack at much lower temperatures. Conceivably thermal shock could crack very badly stressed dice.

So far, six failure mechanisms have been discussed, i.e., 1) fast drift at all temperatures, 2) slow drift at 125°C and higher, 3) films in the region between emitter and base ring at 125°C, 4) emitter shorting at and above 145°C, 5) emitter opens at and above 145°C and 6) cracked dice above 145°C. It is always difficult to establish whether a failure mechanism has a true threshold stress. However, for physical reasons, as discussed above, it is probable that emitters will not open up at temperatures appreciably below 145°C. Failures due to slow drift have so far only been seen at 125°C and higher temperatures. It is virtually certain, though, that they will appear at 95°C as well after a sufficiently long time. Whether emitter shorts and cracked dice will appear below 145°C, or films below 125°C, remains to be seen.

Failure rates normalized to %/1,000 hours have been computed for these tests as a function of time so as to find out whether similar trends occur for storage at 95, 125 and 145°C. Since only one transistor has so far failed at 95°C according to the specified failure criteria, the following tighter criteria were adopted for the purposes of this comparison.

	Initial	Final
Icbo @ 60 V	$\leq$ 2ma	$<$ 3ma
Iebo @ 6 V	$\leq$ 2ma	$<$ 3ma
Ib @ Ic=2a,Vce=2V	$<$ 100ma	$<$ 150ma

Transistors with open emitters were not included in the failure rates. Results are tabulated below.

Time at Lifetest (hrs)	at	Failure Rate in %/1000 Hours 95°C	125°C	145°C
24		----	-----	29.8
72		----	-----	23.2
112		2.54	3.7	21.0
224		----	-----	17.8
336		1.97	1.65	15.9
670		1.35	1.38	----
1000		.98	1.5	----

At all three temperatures, the failure rate decreased with time. However, detailed interpretation in hampered by the fact that even with tightened failure criteria the number of failures at 95°C and 125°C is not large enough. For instance, the failure rates at 112 hours were based on 1 failure out of 350 for the 95°C group and 2 failures out of 500 for the 125°C group.

It is interesting that from 0-670 hours there is virtually no difference between the 95°C and the 125°C groups. In part this is due to the fact that all groups were pre-baked at 125°C prior to the storage tests. In part, it is due to statistical fluctuations. The general picture will become clearer as more life test results become available.

The situation is different if the below failure criteria are used which are identical with the specified criteria in Icbo and Ib and somewhat tighter in Iebo.

	Initial	Final
Icbo @ 60 V	$\leq$ 3ma	$<$ 6ma
Iebo @ 60 V	$\leq$ 3ma	$<$ 6ma
Ib @ Ic=2a, Vce=2V	$\leq$ 100ma	$<$ 150ma

Failure rates, again normalized at %/1,000 hours, are

Storage temperature	95°C	125°C	145°C
Failure rate/1,000 hours	.097%	2.14%	10.7%

The failures are based on the following: at 95°C, 350 transistors at 1000 hours storage, 350 transistors at 670 hours storage, 400 transistors at 336 hours storage for a total of 719,000 transistor hours. At 125°C, 250 transistors at 2000 hours storage and 250 transistors at 1000 hours storage for a total of 750,000 transistor hours. At 145°C, 300 transistors at 336 hours for a total of 102,000 transistor hours.

If the failure rate for the group at 125°C had been computed at the 1000 hours storage point for all 500 transistors (500,000 transistor hours) the result would have been .82%/1000 hours. Thus, the failure rate increases drastically beyond 1000 hours of storage. The increase in failure rate is due in part to units drifting gradually out of specification. Irrespective of which figures are used, it is evident that the failure rates on our transistors increase rapdily with storage temperature. In part, the rate of increase is associated with the desiccant (see Section III-4), and it will be interesting to find out whether the rate can be reduced by the use of different dessicants such as molecular sieve.

Twenty-four transistors from the same lot of 3,000 transistors were put on a step-stress test. The stress was temperature, the steps being 20°C, starting at 140°C and running to 240°C. The transistors were held at each temperature for 22 hours. Temperature was controlled to ± 1°C. Since indium melts at 155°C, transistors were not moved from the oven until they had cooled to well below that temperature. The following failure criteria were used:

Icbo @ 60 V $\geq$ 6ma

Iebo @ 60 V $\geq$ 6ma

Ib @ Ic=2a, Vec=2V $\geq$150ma

Exhibit 44 is a plot on probability paper of failure rate versus 1/T. The data can be fitted quite well by a straight line indicating that substantially the same failure modes are encountered in the temperature range 140°C - 240°C. Failure analysis indicated that two transistors had cracked dice at the end of the test. A breakdown of defectives at given temperature is given below by Icbo, Iebo and Ib.

Temperature, 0°C	Icbo/60V	Iebo/60V	Ib/Ic=2a
140	----	----	----
160	1	----	----
180	6	1	----
200	10	1	2
220	12	6	2
240	17	9	2

This illustrates vividly that at this time the collector and emitter junctions are a far greater source of failure than Ib. The same conclusion is drawn from the breakdown of defectives after 336 hours at 145°C, i.e., omitting the open emitter failure, there were 11 failures in Icbo, 9 failures in Iebo and only 1 failure in Ib.

In these as well as in other storage life tests, attempts have been made to find a correlation between initial distribution and the failure rate. Such attempts have invariably been unsuccessful. For instance, in one experiment (#17) consisting of 340 units, 34 developed Ico's $\geq$ 4ma at 60 volts during 333 hours of storage at 145 C. These "failures" had at zero hour a

median value of 0.25ma and a distribution very similar to that for the total 340 units. Again in another experiment (#13) in which sealing was done in two stages, those units sealed in the first stage show a better zero hour distribution than those sealed in the second stage. However, after storage for 168 hours at 145°C there are a significantly larger number of failures among the second lot. Thus, the failure rate does not depend on the initial Ico distribution.

IV CONCLUSIONS

The following conclusions are drawn from the work during the third quarter.

1. At the end of the second quarter we stated that in the comparison between conventionally rinsed and jet rinsed transistors no significant differences were observed as far as initial (i.e., prior to life test) distributions of electrical parameters were concerned. It is now conlcuded that the same is true in regard to performance during 145°C storage test.

2. Bakes prior to encapsulation in dry oxygen at 100°C give superior results both, initially and during storage test, in that frequency distributions of electrical parameters are tighter and fewer failures are generated. Bakes in dry nitrogen produce almost as tight distributions but result in more failures. Bakes in dry ambients at 150°C and bakes in wet ambients at 100°C tend to produce higher leakage and more scattered distributions.

3. Transistors were coated with silane by the method described in the second quarterly report. Coated and uncoated transistors have very similar distributions of electrical parameters before life test. During storage at 145°C, the gain of coated transistors tends to increase while the gain of non-coated transistors generally decreases. As far as emitter and collector leakage are concerned, no difference is discernible between coated and uncoated units.

4. Coated and non-coated transistors show distinctly different behavior when exposed to a high relative humidity ambient. Leakage of coated units tends to remain the same as in a dry ambient while the leakage of uncoated units increases on the average. However,

these trends are far from uniform. Some uncoated transistors hardly change on transfer from the dry to the wet ambient and, in general, the effect of humidity is far greater on the collector junction than on the emitter junction.

5 A novel method of introducing helium into the package for purposes of leak detection represents a substantial improvement over the previously used method and will be incorporated into production as soon as the equipment becomes available.

6 It was discovered that our desiccant, calcium sulphate, sometimes behaves erratic, and steps have been taken to control it more closely. Very encouraging results have been obtained with molecular sieve both, initially and particularly during high temperature storage.

7 An internal clip of new design has been compared with our present clip. We conclude that the new design greatly improves the alignment of the die on the dimple. However, there is still some difficulty due to non-uniform electro-plated tinning of the clip which results in poor soldering between clip and base ring. A batch of tin-clad clips is on order. In addition it was found that a further improvement results from placing weights on the clips during soldering.

8 From a comparison of collector pellets, 5 mils and 10 mils thick, it is concluded that the latter alloy more easily. On the average, therefore, 10 mils thick pellets produce more uniform junctions than the 5 mils thick pellets which are now being used. Electrically, the more uniform junctions result in fewer hot spots, fewer abnormally high fLoating potentials and probably also in lower leakage, though evidence on the latter point is not conclusive presumably on account of masking effects.

9 Storage test data at 95°C, 125°C and 145°C have been accumulated for a homogeneous lot of 3,000 transistors. Using the failure criteria

Icbo @ 60 V $\geqslant$ 6ma

Iebo @ 60 V $\geqslant$ 6ma

Ib @ Ic=2a, Vce=2V $\geqslant$ 150ma

we find the following approximate failure rates

Storage Temperature °C	Failure Rate %/1000 hours	Transistor-Hours
95	.1	719,000
125	1.0	500,000
145	11.0	102,000

At all these temperatures the normalized failure rates decrease during the first four hundred hours of storage. At 125°C, the failure rate goes through a minimum at about 700 hours, and then increases with time. Similar effects will undoubtedly show up at other storage temperatures as well.

10 Failure analysis revealed a number of failure modes such as "slow" and "fast" drift, conductive films in the region between emitter and base ring, shorted emitters, opening of the solder joint between emitter and tab and between base ring and tab, and cracked dice. Some of these modes have so far only been observed at relatively high storage temperatures.

The most common failure mode at 125°C is "fast" drift. At 95°C only one failure has so far been observed and hence no general statements can be made. For a discussion of failure modes at higher storage temperatures refer to the text.

V PROGRAM FOR NEXT QUARTER

1. Initial and life test data indicate that jet rinsing is either ineffective or that its effects are being masked. Hence, no further work on jet-rinsing is planned for the next quarter. Instead, we will work towards an improvement of our etching procedure.

2. Bakes in dry oxygen at 100°C have given superior results. Further work along these lines is planned, and on the basis of further data a decision will be made as to whether the process will be incorporated into production.

3. Transistors will be silane-coated according to the new procedure described in the text, and results will be evaluated.

4. Further efforts will be made to tighten control on our present dessicant. In addition, pilot runs are planned with molecular sieve. At the end of the fourth quarter it should be possible to make a decision as to which of the two dessicants is to be used in production.

5. Several pilot runs are planned with the redesigned clip. If the early favorable results are confirmed, then it is anticipated that the new clip will become a standard piece part during the fifth quarter.

6. Six pilot runs are being run in a comparison of our present 5 mil thick collector and the proposed 10 mil thick collector. If the early favorable results are reproduced, preparation for a switch-over will be made during the latter part of the fourth quarter, and the 10 mil thick collector will become a standard piece part during the fifth quarter.

7 Some changes in the handling of piece parts and sub-assemblies will be made during the fourth quarter. This represents, of course, a continuing program, and further changes during the later quarters are to be expected.

8 Equipment for helium leak detection in on order and the improved procedure described in the text will be introduced during the fourth quarter.

VI PUBLICATIONS AND REPORTS

No publications and reports have resulted from or about this contract.

VII IDENTIFICATION OF TECHNICIANS

No changes in personnel occurred as between the second and third quarter.

Engineering Hours

During the quarter, 1,287 hours were expended by salaried personnel; 921 hours were expended by hourly personnel.

VIII LIST OF FIGURES

transistors shown in Exhibit 6-A.

Exhibit 7-B Distributions of Iebo at 333 hours of 145°C storage for the three groups of transistors shown in Exhibit 6-A.

8-A Distributions of Icbo at 0 hours for two groups of transistors: units baked in dry oxygen at 100°C and units baked in wet oxygen at 100°C.

8-B Distributions of Icbo at 333 hours of 145°C storage for the two groups of transistors shown in Exhibit 8-A.

9-A Distributions of Iebo at 0 hours for the two groups of transistors shown in Exhibit 8-A.

9-B Distributions of Iebo at 333 hours of 145°C storage for the two groups of transistors shown in Exhibit 8-A.

10 Percentage of transistors having Icbo $>$ 1 ma @ 60 volts for 11 groups which were welded consecutively.

11 Distributions of Icbo at 0, 168 and 333 hours of 145°C storage for two consecutively welded groups of transistors denoted as Seal 1 and Seal 2.

12-A Distributions of Icbo at 0 hours for two consecutively welded groups of transistors denoted as Seal 1 and Seal 2.

12-B Distributions of Icbo at 168 and 333 hours of 145°C storage for the two groups of transistors shown in Exhibit 12-A.

13 Distributions of Icbo and Iebo for transistors after burn-in and after a subsequent half minute etch.

14 Distributions of Icbo for two groups of transistors before welding and after burn-in. One group was etched 1½ minutes and the other group was etched in steps of 1½ minutes plus

an additional ½ minute.

Exhibit 15 Distributions of Iebo at zero hours for two groups of transistors: controls and silane coated units.

16 Distributions of Iebo at 100 hours of 145°C storage for the same groups of transistors shown in Exhibit 15.

17 Distributions of Icbo at zero hours for the same groups of transistors shown in Exhibit 15.

18 Distributions of Icbo at 100 hours of 145°C storage for the same groups of transistors shown in Exhibit 15.

19 Distributions of Ib at 0 and 344 hours of 145°C storage for a silane coated and a control group of transistors.

20 Distributions of Icbo and Iebo at zero hours for a silicate coated and a control group of transistors.

21 Distributions of Icbo and Iebo at 344 hours of 145°C storage for the two groups shown in Exhibit 20.

22 Distributions of Ib at 0 and 344 hours of 145°C storage for the groups shown in Exhibit 20.

23 Scattergram of Icbo in a dry and wet ambient.

24 Scattergram of Icbo readings after 145°C storage and after additional 30 days of room temperature storage.

25 Distribution Normality Test of Icbo at 0, 100 and 270 hours of 145°C storage.

26 Distributions of Icbo and Ib for two groups of transistors: units containing $CaSO_4$ and units containing molecular sieve pellets.

27-A Average Icbo and Iebo as a function of storage time at 145°C for transistors containing $CaSO_4$ and transistors containing

molecular sieve pellets.

Exhibit 27-B Average Ib as a function of storage time at 145°C for the groups of transistors shown in Exhibit 27-A.

28-A Distributions of Icbo at 0, 48, 168 and 333 hours of 145°C storage for the transistors containing $CaSO_4$ which were shown in Exhibit 27-A.

28-B Distributions of Icbo at 0, 48, 168 and 333 hours of 145°C storage for the transistors containing molecular sieve pellets which were shown in Exhibit 27-A.

29 Drawing of redesigned internal clip.

30 Drawing of redesigned internal clip modification. The tip of the emitter tab is bent 90°.

31 Drawing of a jig designed to fuse the clip.

32 Drawing of a jig designed to test open transistors.

33 Distributions of Icbo and Iebo at 0, 112, 336, 670 and 1000 hours of 95°C storage.

34 Distributions of Icbo and Iebo at 0, 112, 336, 670 and 1000 hours of 125°C storage. Transistors are from the same homogeneous lot as those in Exhibit 33.

35 Distributions of Icbo and Iebo at 0, 24, 72, 112, 224 and 336 hours of 145°C storage. Transistors are from the same homogeneous lot as those in Exhibit 33.

36 Median Icbo versus storage time at 95°C, 125°C and 145°C. The medians were calculated from the data shown in Exhibits 33 to 35.

37 Median Iebo versus storage time at 95°C, 125°C and 145°C. The medians were calculated from the data shown in Exhibits 33 to 35.

Exhibit 38 Readings of Icbo and Iebo versus time for the transistors which failed during 1000 hours of 125°C storage. The data are derived from Exhibit 34.

39 Readings of Icbo and Iebo versus time for the transistors which failed during 333 hours of 145°C storage. The data are derived from Exhibit 35.

40 Distribution Normality Test of Icbo at 100 and 336 hours of 145°C storage. The data are derived from Exhibit 35.

41 Distributions of Icbo and Iebo before storage, after 145°C storage and after a half minute etch subsequent to storage.

42 Microphotograph of a strand of indium bridging the emitter junction. Also shown are two incipient strands of indium.

43 Microphotograph showing details of a strand of indium which bridges the emitter junction.

44 Plot of accumulative failure rate versus 1/T for a step-stress test of transistors from the same homogeneous lot as those in Exhibit 33.

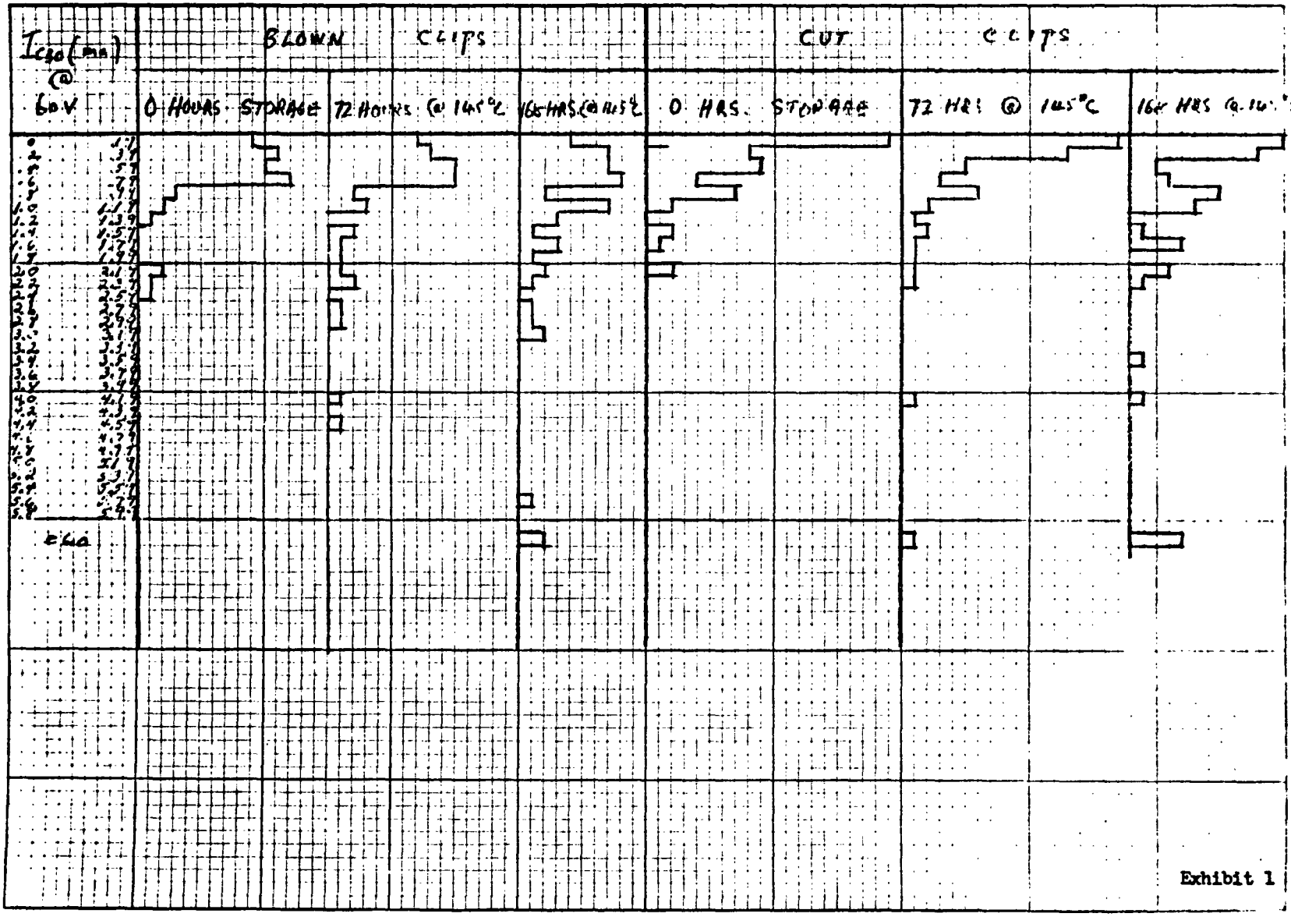

I_{C40} (mA) @ 60V
BLOWN CLIPS
0 HOURS STORAGE
72 HOURS @ 145°C
168 HRS @ 145°C
CUT CLIPS
0 HRS. STORAGE
72 HRS @ 145°C
168 HRS @ 145°C

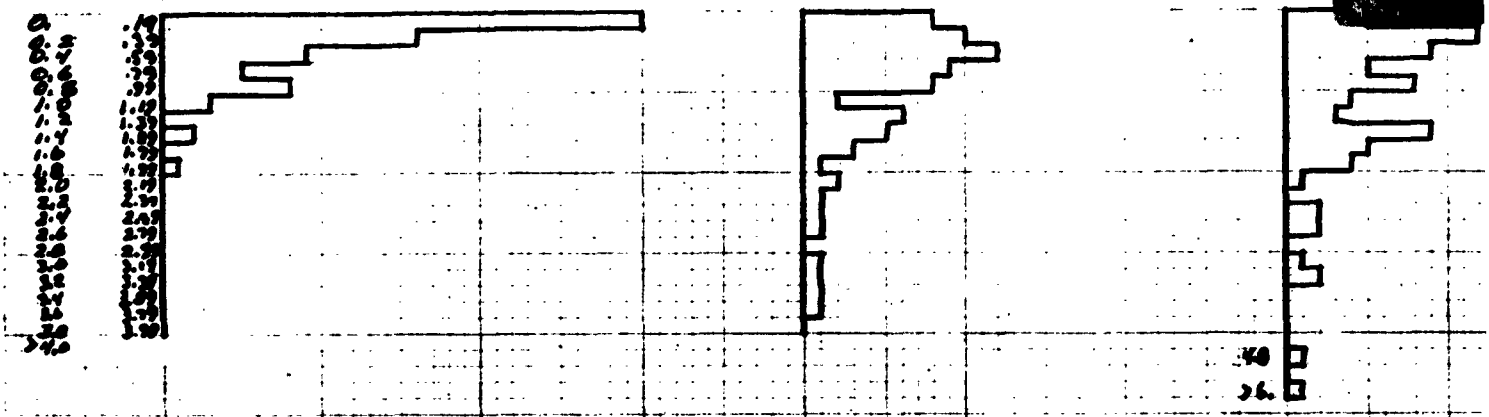
Exhibit 1

Rinsing complete when resistivity of outlet water equals resistivity of in

I_{CBO} @ 60V (na)

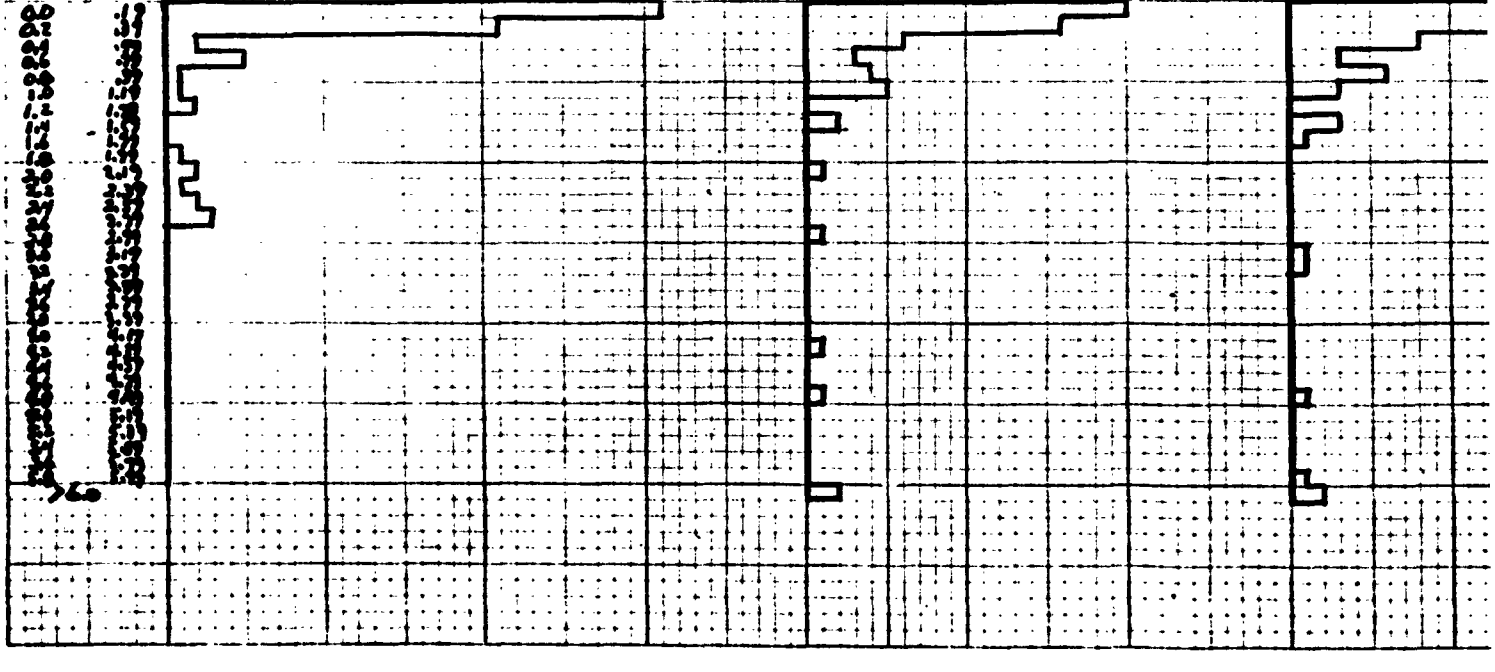
0 Hrs Storage

168 Hrs @ 145°C



Comparison with the 10 second rinse on sheet 16.2 shows no obvious distinction for either the I_{CBO} or I_{EBO} distributions

I_{EBO} @ 60V (ma)

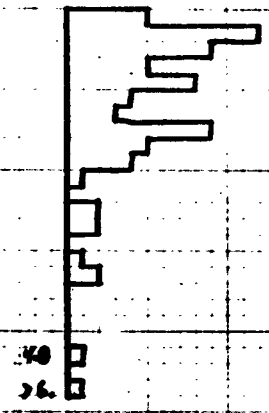


als resistivity of inlet

@ 145 °C

333 Hrs @ 145 °C

2



on sheet 16.2 shows

e IC30 or IEB0 distributions

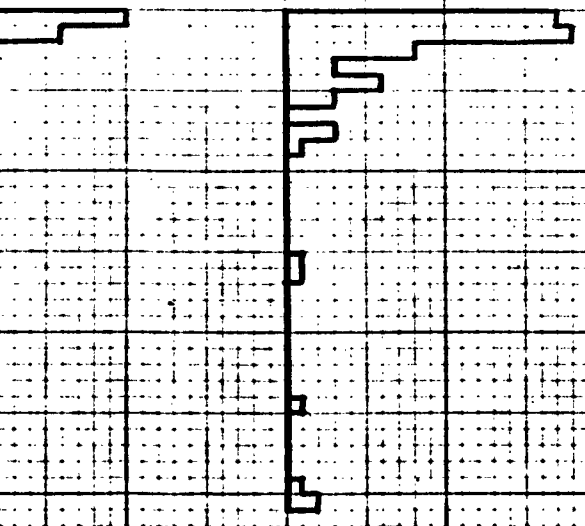
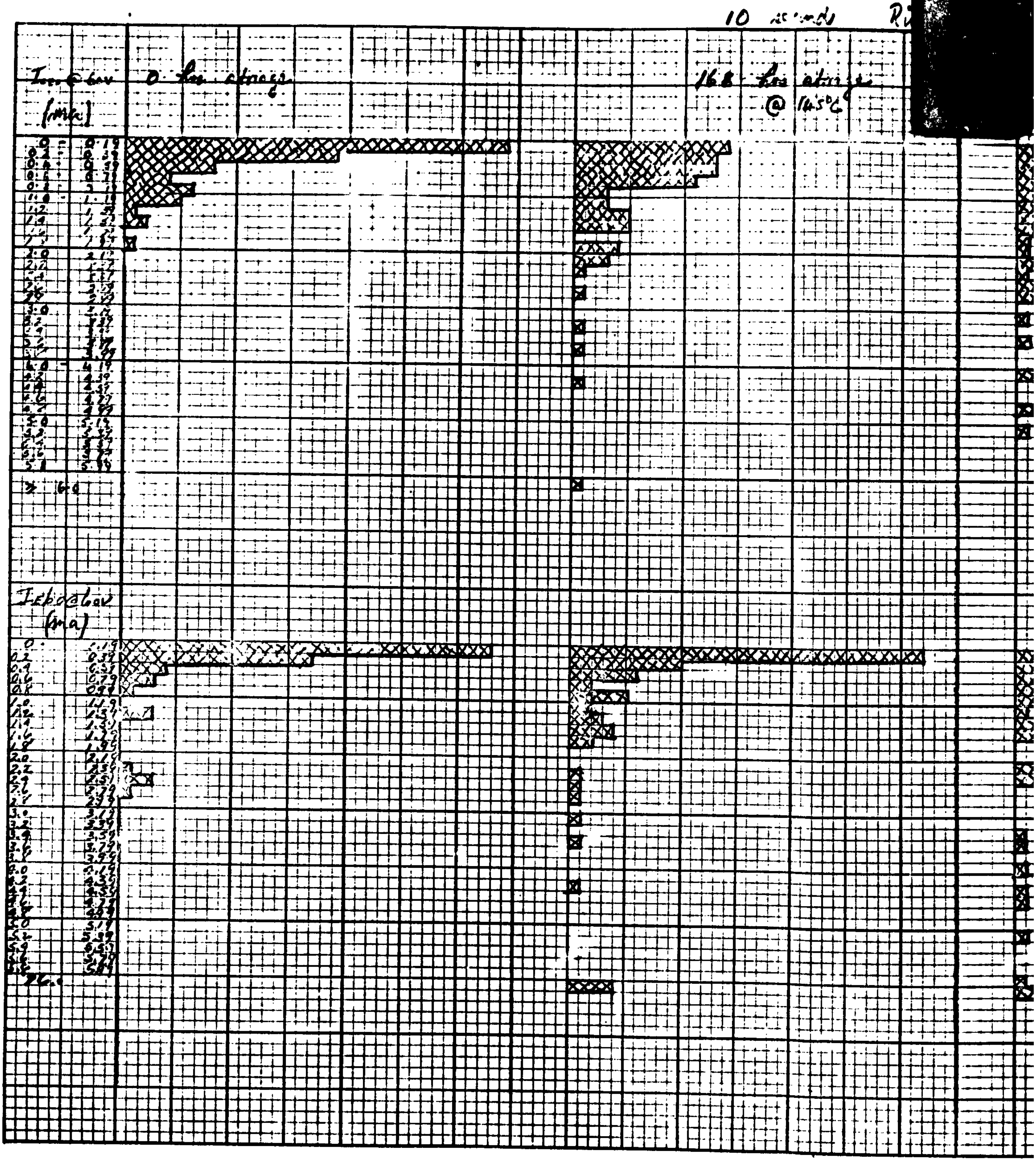


Exhibit 2-A



10 seconds
0 hrs storage
168 hrs storage
@ 145°C
(mA)
(mA)

10 second Rinse.

168 hr. storage @ 14.5°C

336 hr. @ 14.5°C

2

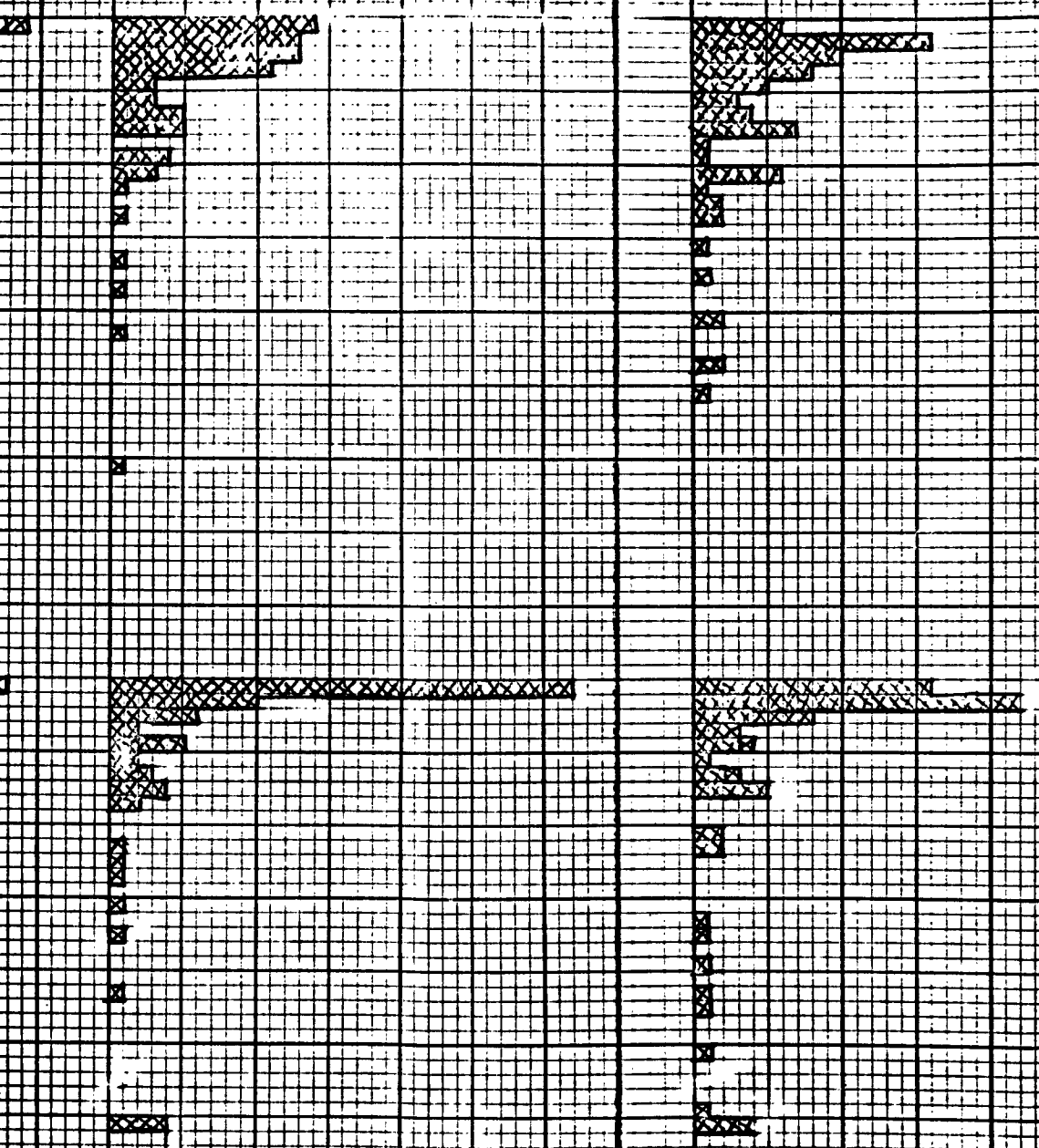
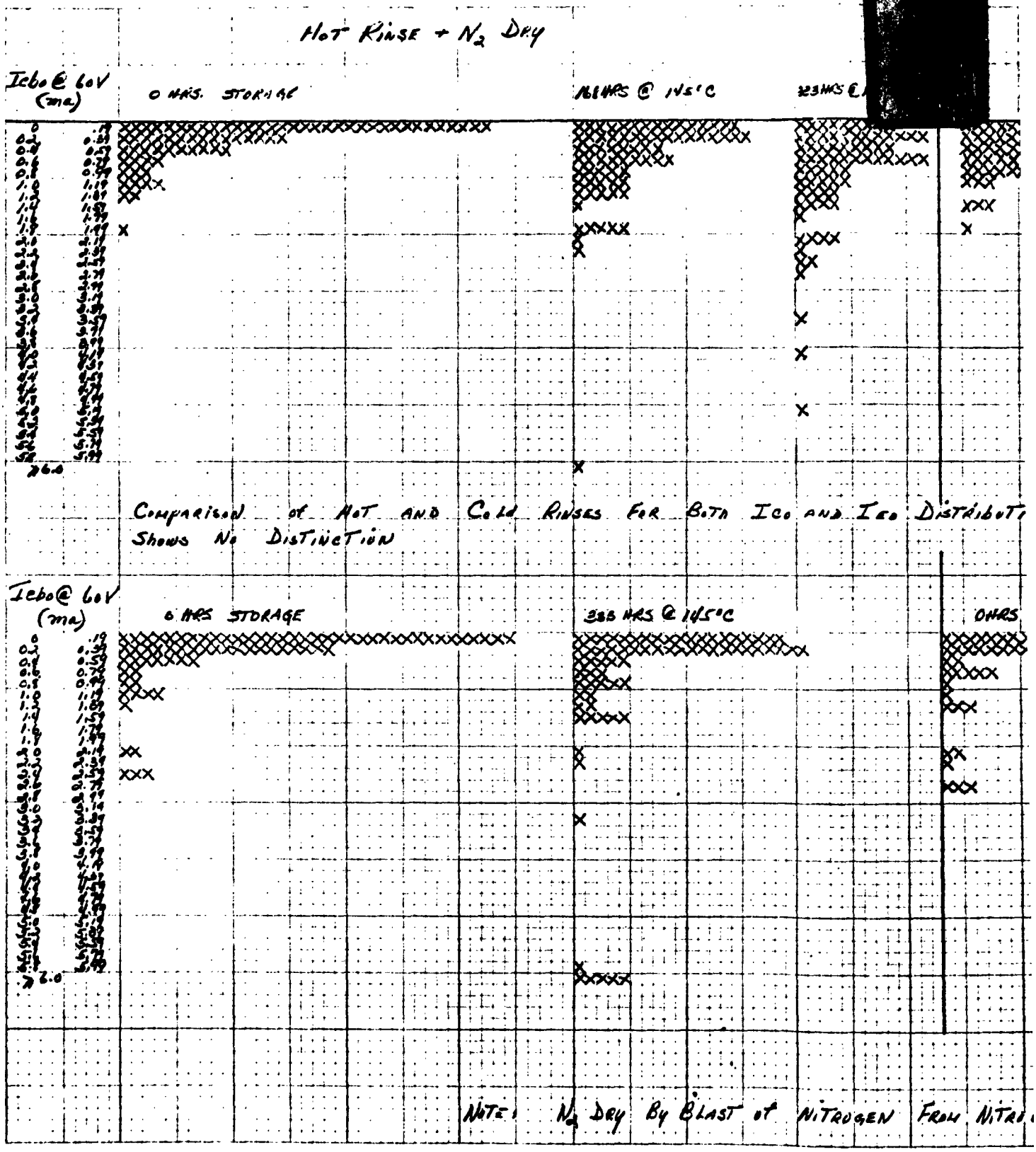
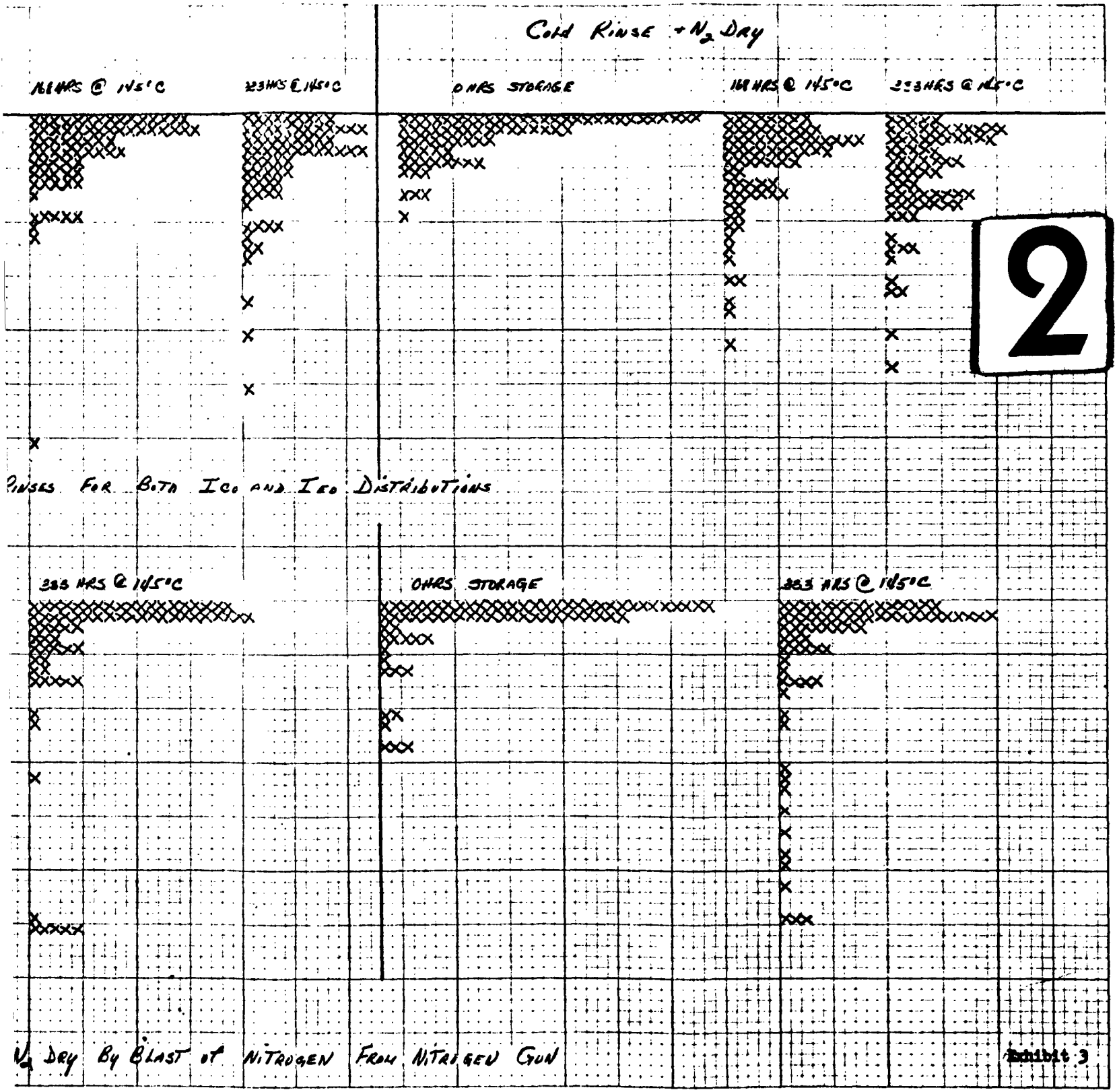


Exhibit 2-3


Hot Rinse + N_2 Dry
Icbo @ 60V (ma)
0 HRS. STORAGE
Comparison of Hot and Cold Rinses for Both Icbo and Icbo Distributi
Shows No Distinction
Icbo @ 60V (ma)
0 HRS STORAGE
238 HRS @ 145°C
0 HRS
Note: N_2 Dry By Blast of Nitrogen From Nitro

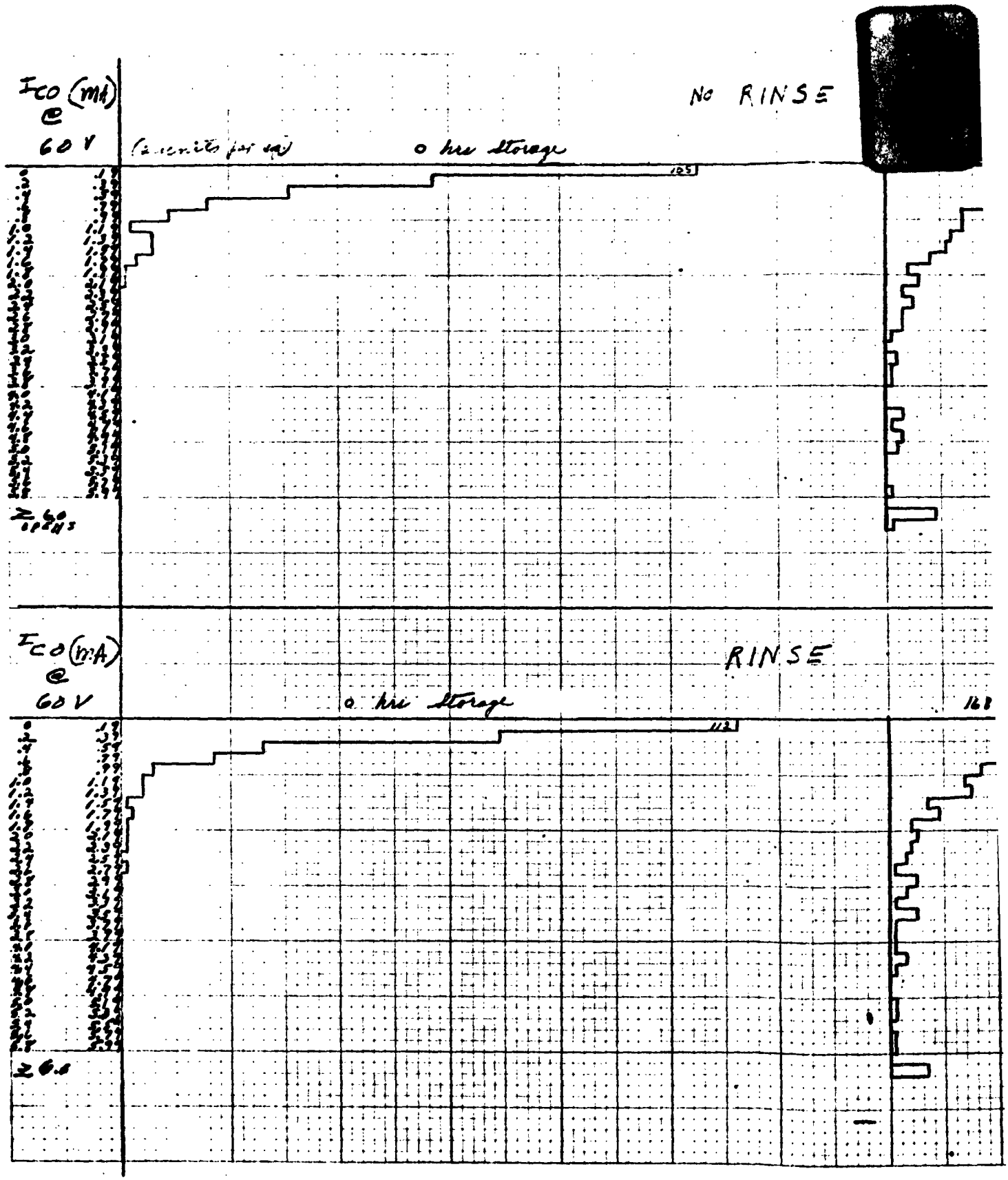
Cold Rinse + N_2 Dry



Rinses For Both I_{CO} and I_{EO} Distributions

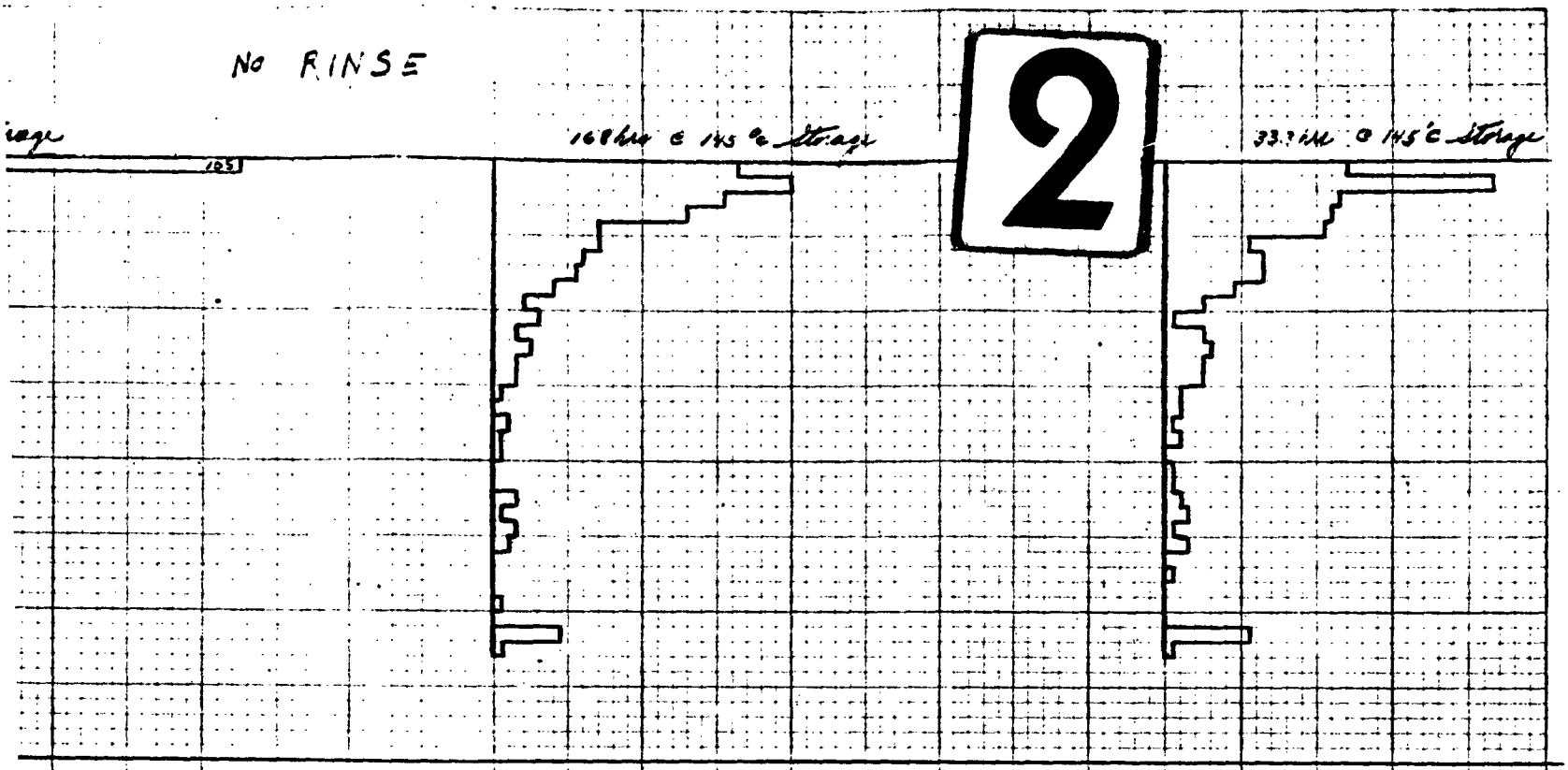
N_2 Dry By Blast of Nitrogen From Nitrogen Gun

Exhibit 3


I_{CO} (mA) @ 60 V
NO RINSE
0 hrs storage
125
I_{CO} (mA) @ 60 V
RINSE
0 hrs storage
112

NO RINSE

2



RINSE

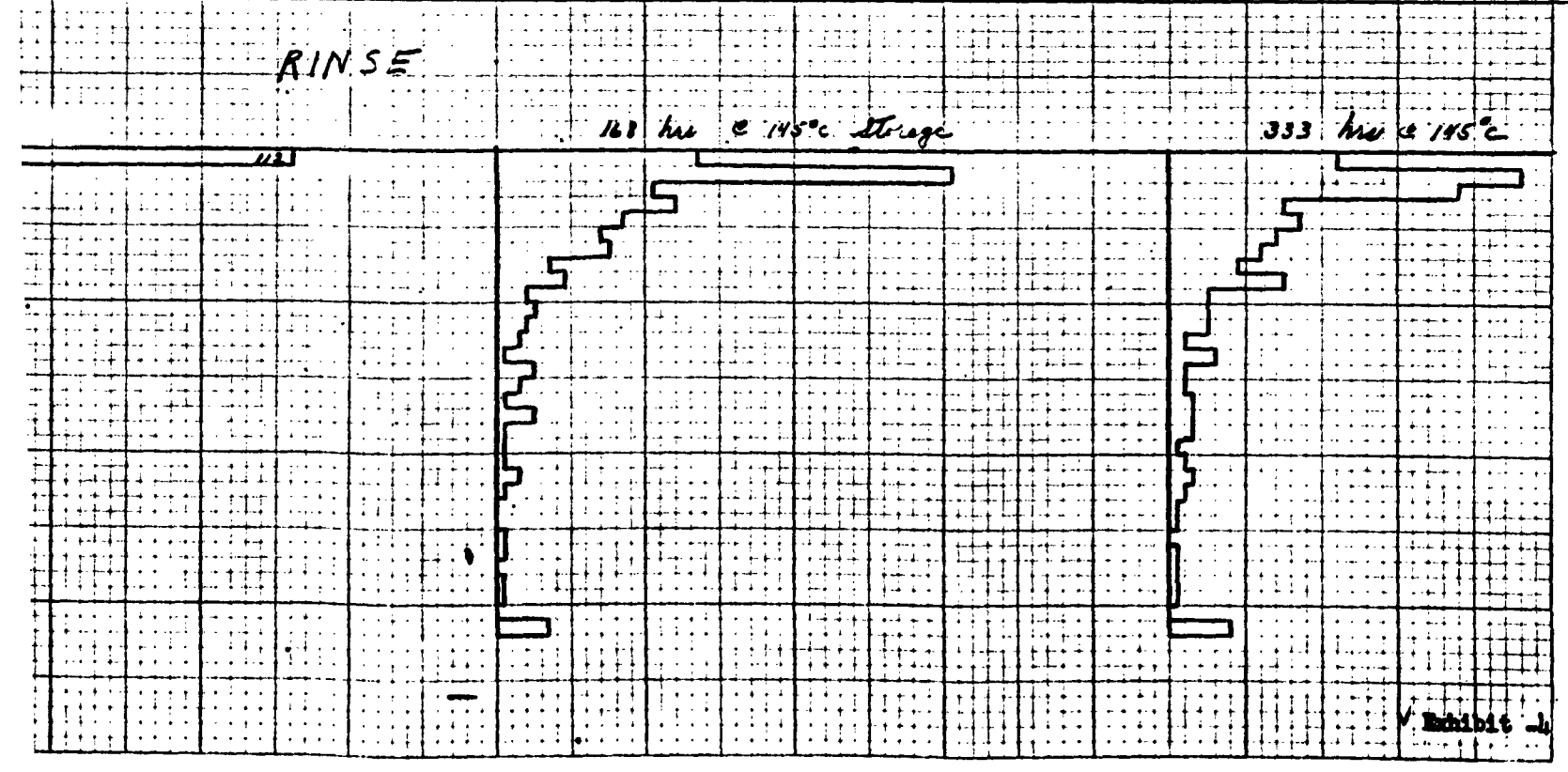


Exhibit 4

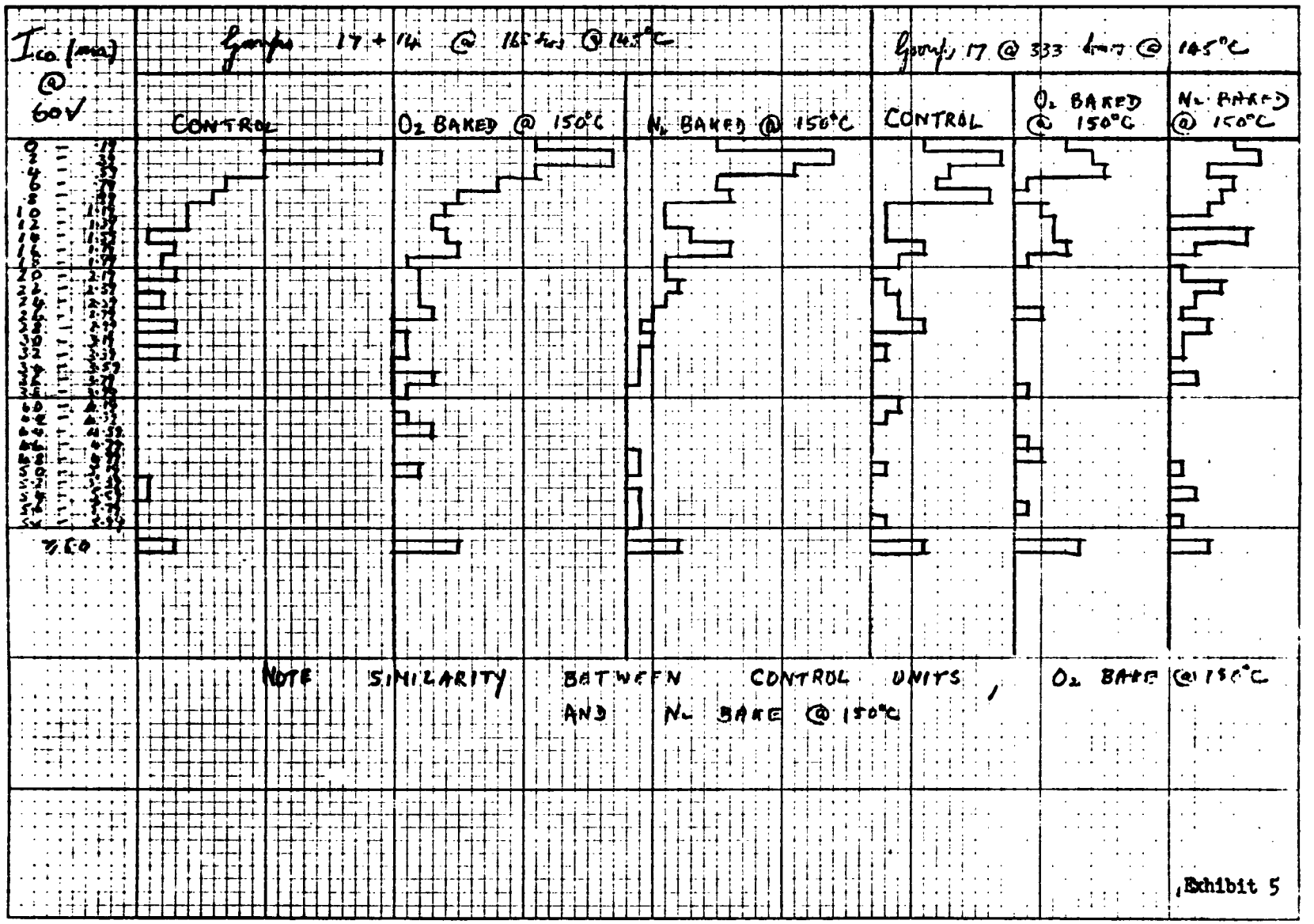
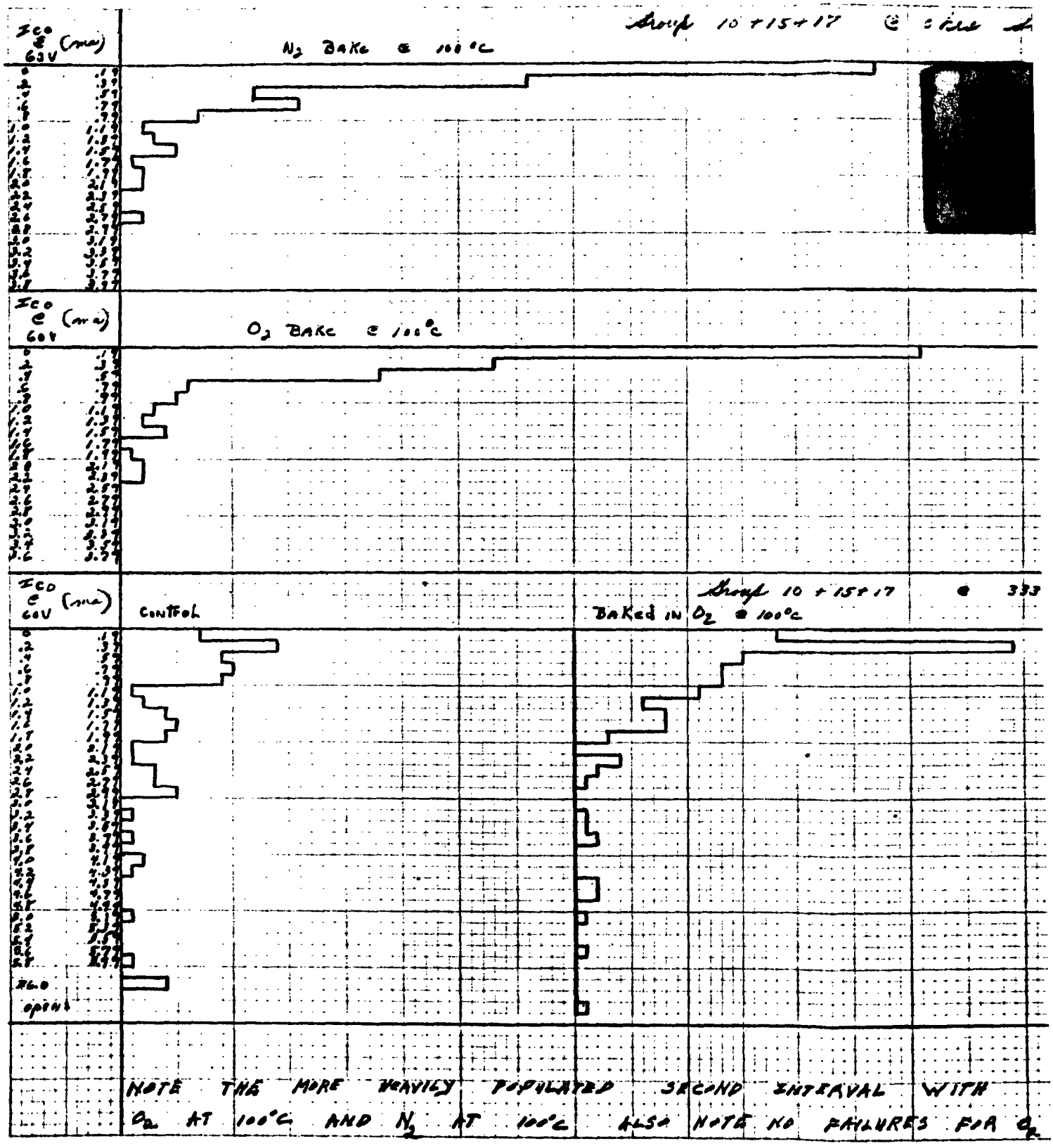

I_{CO} (max) @ 60V
Groups 17 + 14 @ 165 hrs @ 145°C
Groups 17 @ 333 hrs @ 145°C
CONTROL
O_2 BAKED @ 150°C
N_2 BAKED @ 150°C
CONTROL
O_2 BAKED @ 150°C
N_2 BAKED @ 150°C
0 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38 40 42 44 46 48 50 52 54 56 58 60
% CO
NOTE SIMILARITY BETWEEN CONTROL UNITS, O_2 BAKED @ 150°C AND N_2 BAKED @ 150°C

Exhibit 5


I_{CO} @ 60V (ma)
N_2 BAKE @ 100°C
O_2 BAKE @ 100°C
CONTROL
BAKED IN O_2 @ 100°C
NOTE THE MORE HEAVILY POPULATED SECOND INTERVAL WITH O_2 AT 100°C AND N_2 AT 100°C ALSO NOTE NO FAILURES FOR O_2

Group 10 + 15 + 17 @ 333 hrs Storage

CONTROL

2

Exhibit 6-A

Group 10 + 15 + 17 @ 333 hrs @ 145 C Storage

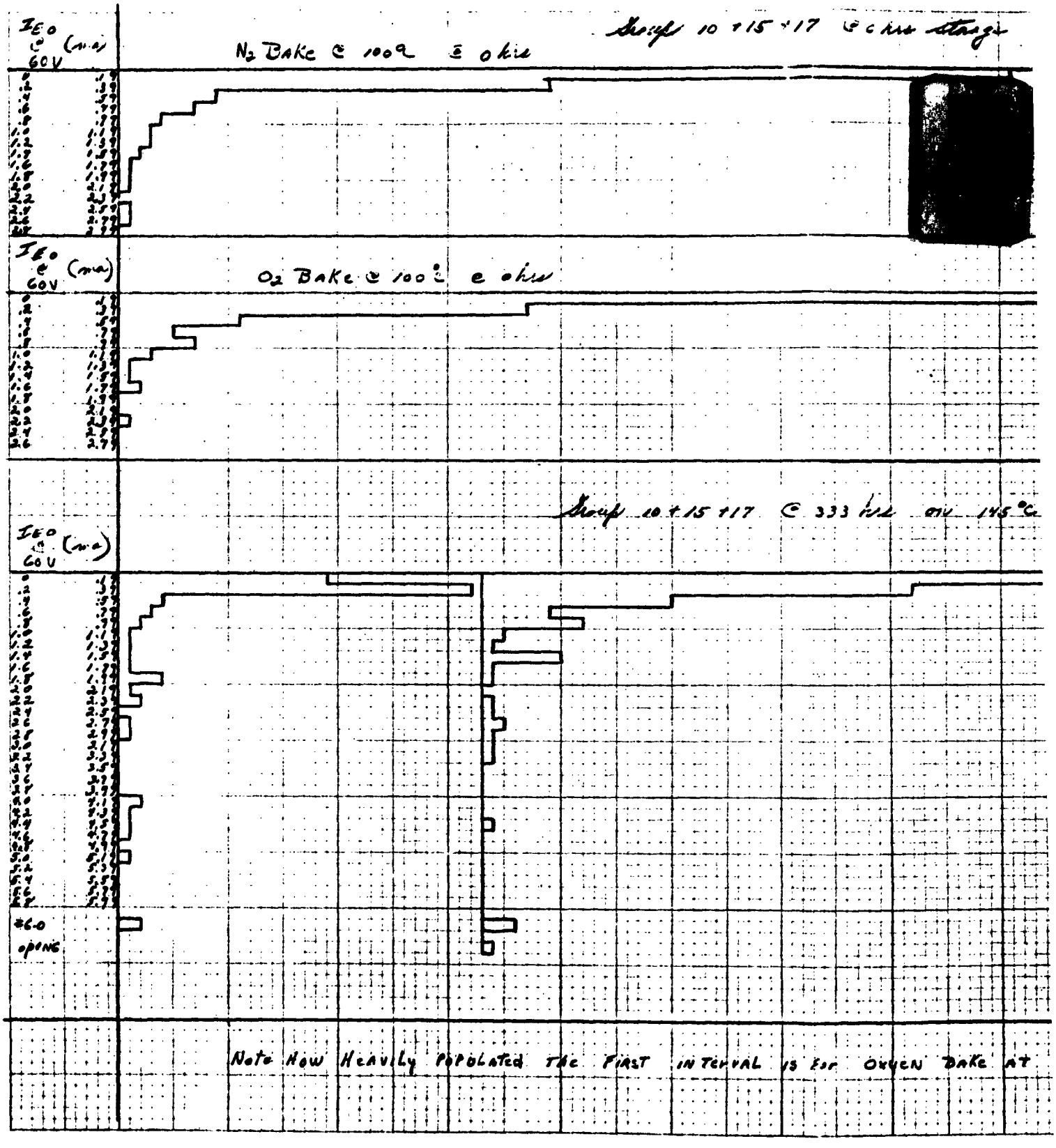
BAKED IN O_2 @ 100°C

BAKED IN N_2 @ 100°C

Exhibit 6-B

ED SECOND INTERVAL WITH

ALSO NOTE NO FAILURES FOR O_2 AT 100°C EXCEPT ONE OPEN


I_{E_0} @ 60V (ma)
N_2 Bake @ 100° C ohrs
Groups 10 + 15 + 17 @ ohrs storage
I_{E_0} @ 60V (ma)
O_2 Bake @ 100° C ohrs
Groups 10 + 15 + 17 @ 333 hrs ATV 145°C
I_{E_0} @ 60V (ma)
#6-0 spring
Note how heavily populated the first interval is for oxygen bake at

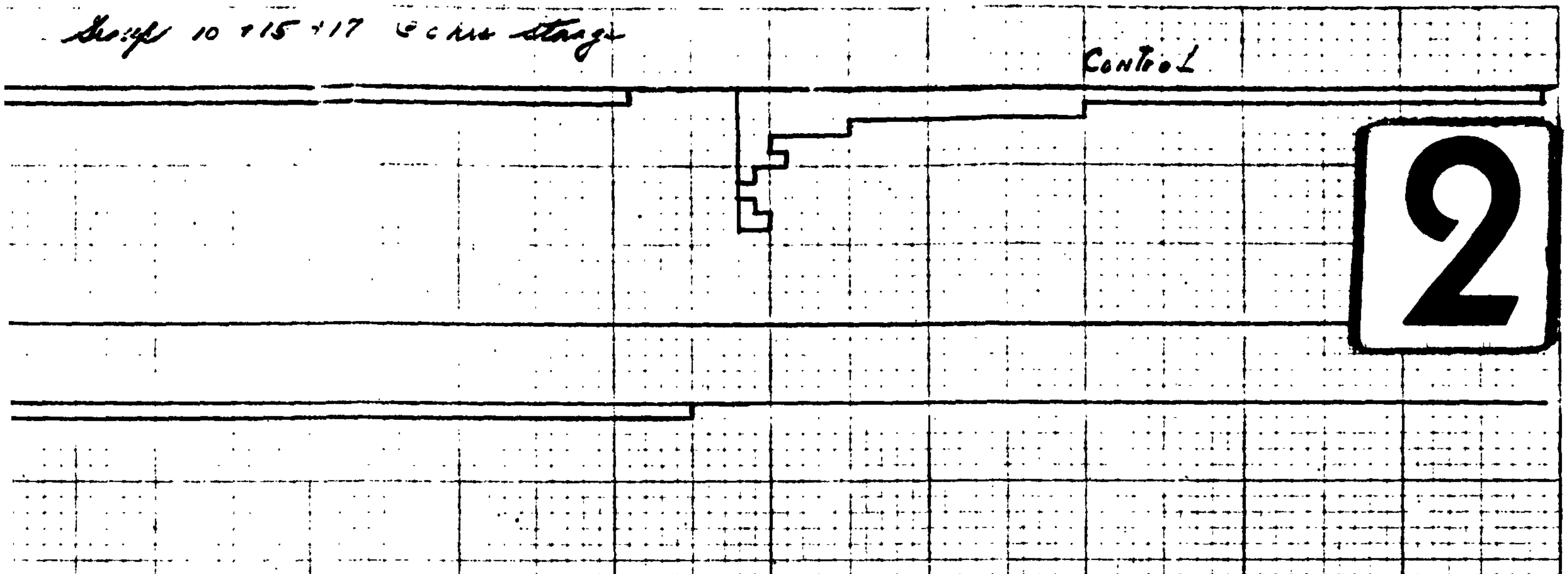


Exhibit 7-A

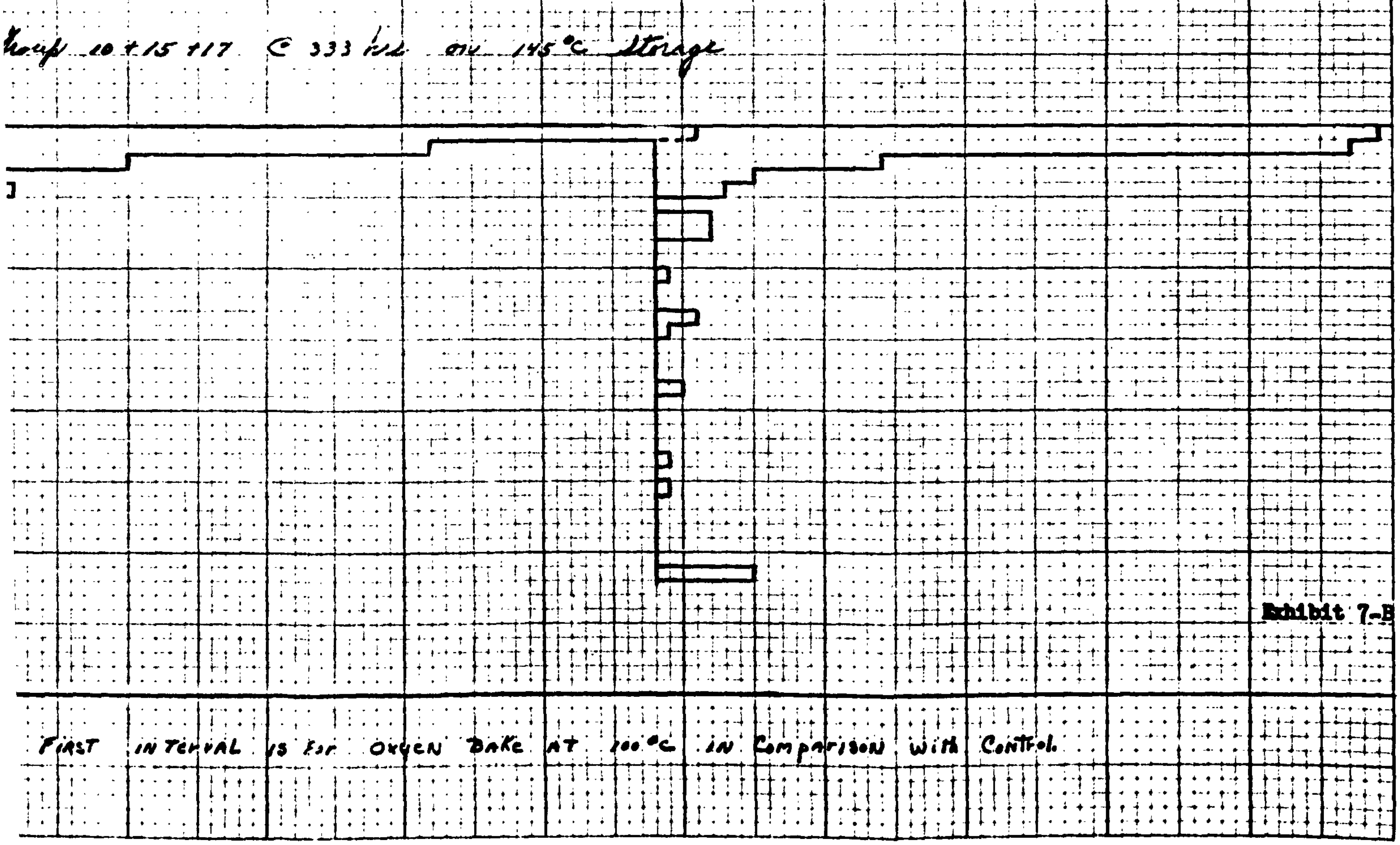
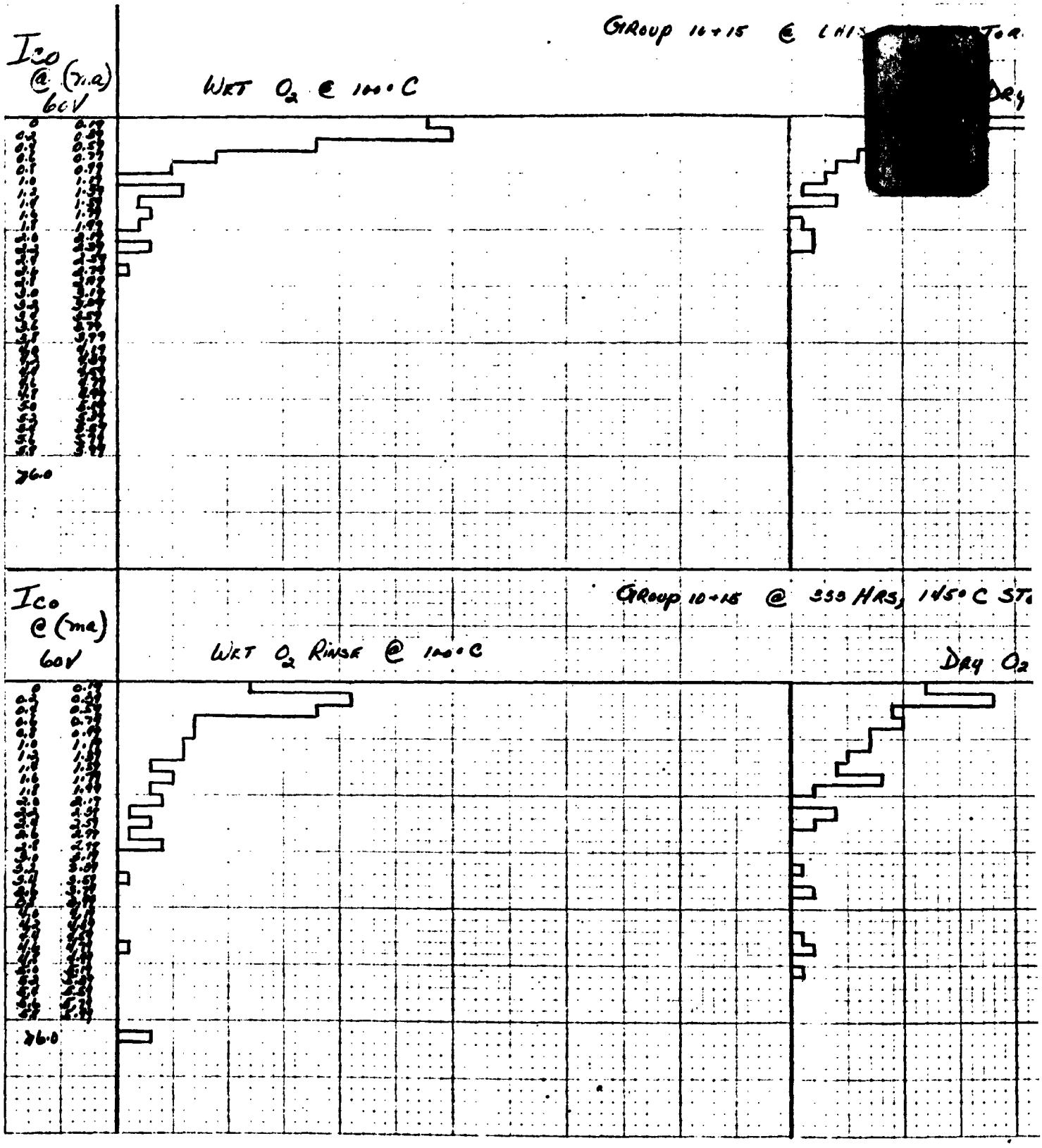


Exhibit 7-B



GROUP 10-15 @ 0 HRS, 145°C STORAGE

Dry O_2 @ 100°C

2

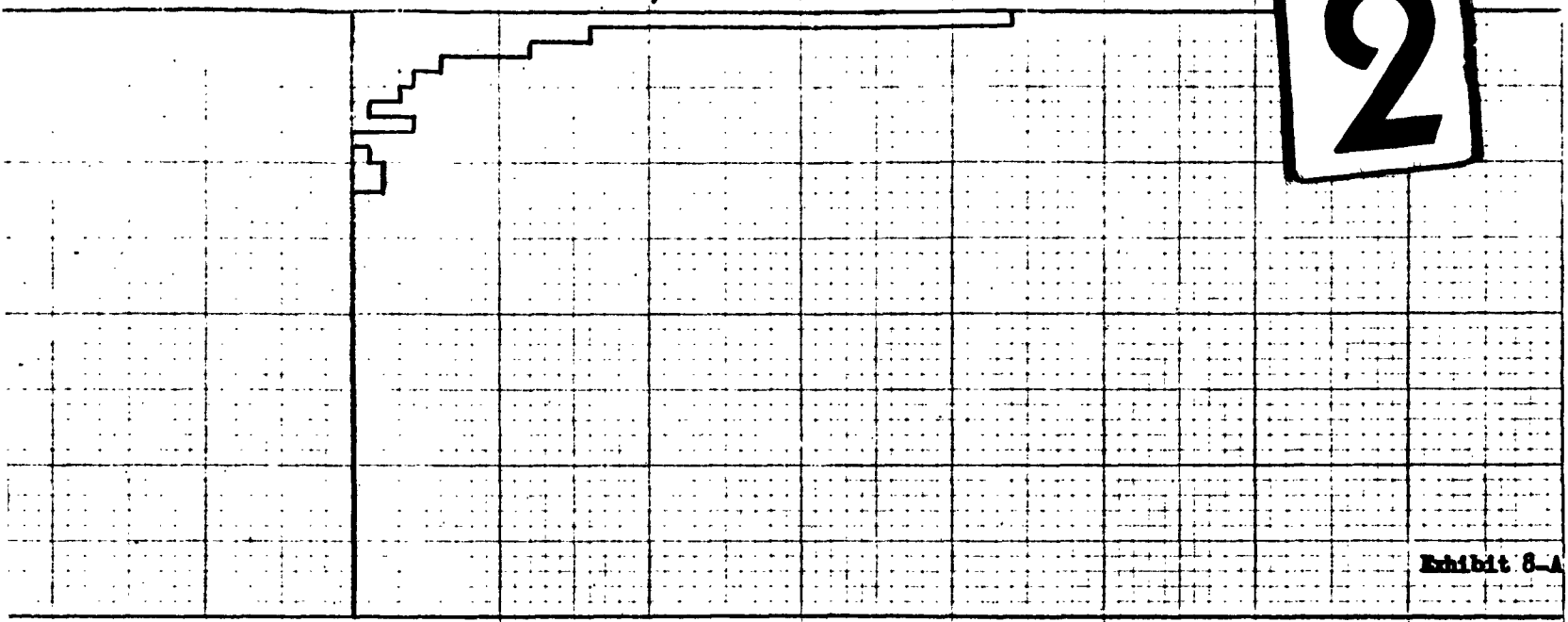


Exhibit 8-A

GROUP 10-15 @ 338 HRS, 145°C STORAGE

Dry O_2 RINSE @ 100°C

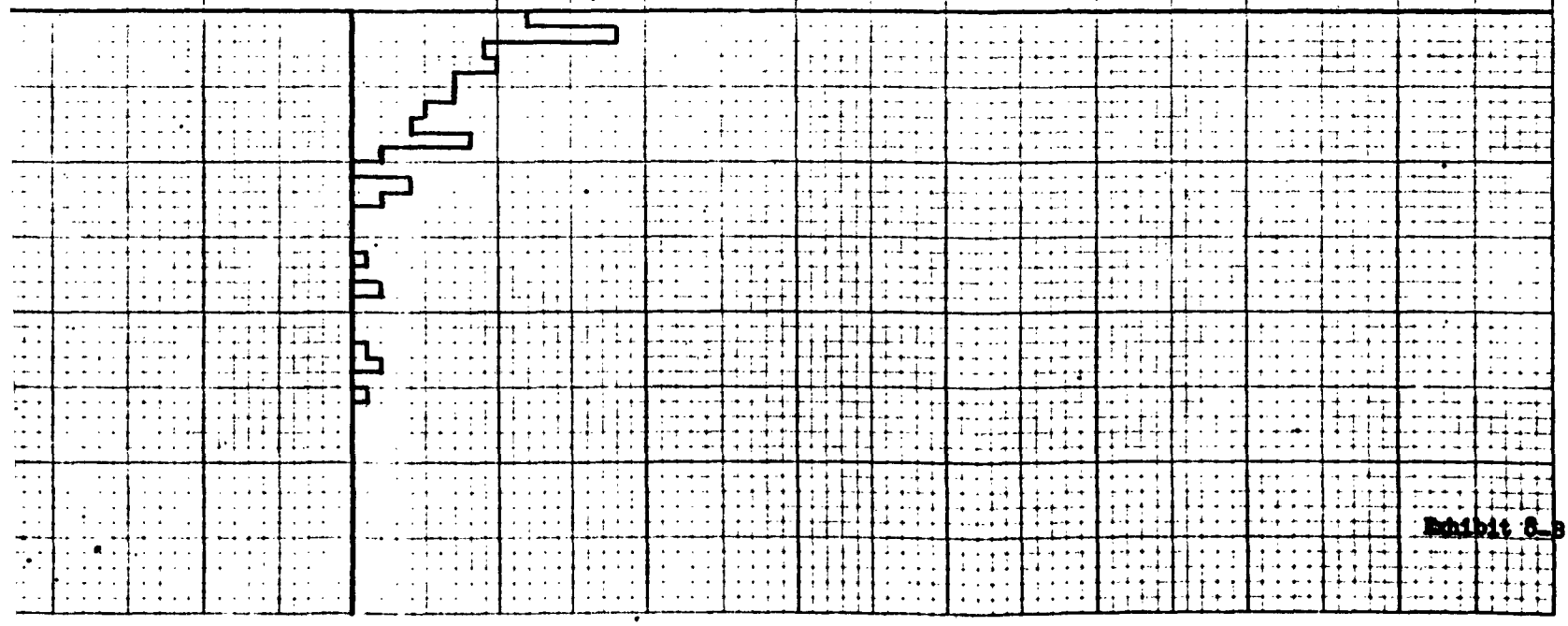
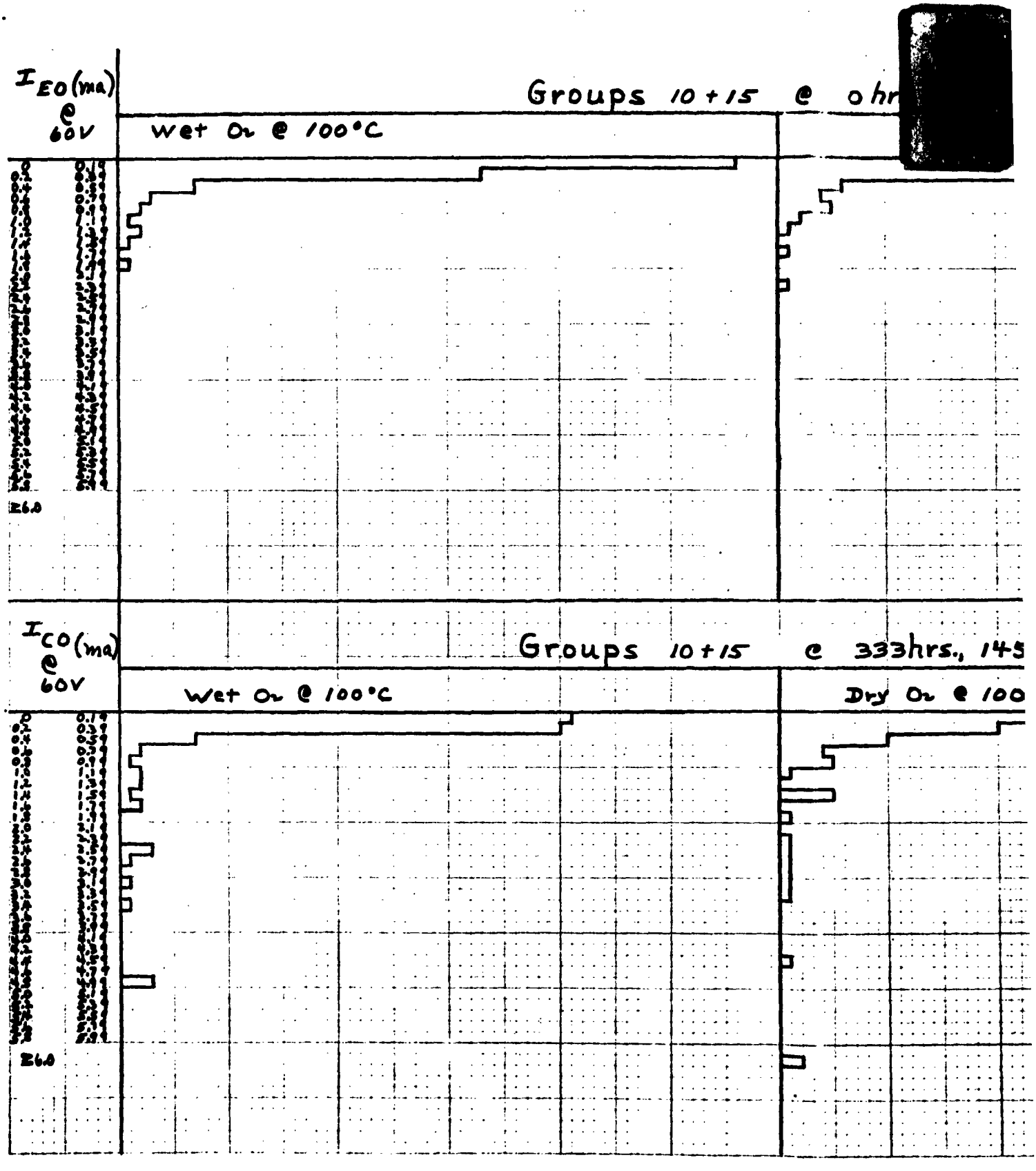


Exhibit 8-B


I_{EO}(ma) @ 60V
Groups 10+15 @ 0 hr
Wet O₂ @ 100°C
E6.0
I_{CO}(ma) @ 60V
Groups 10+15 @ 333hrs., 145
Wet O₂ @ 100°C
Dry O₂ @ 100
E6.0

roups 10+15 @ 0 hrs., 145°C storage

Dry Oz @ 100°C

2

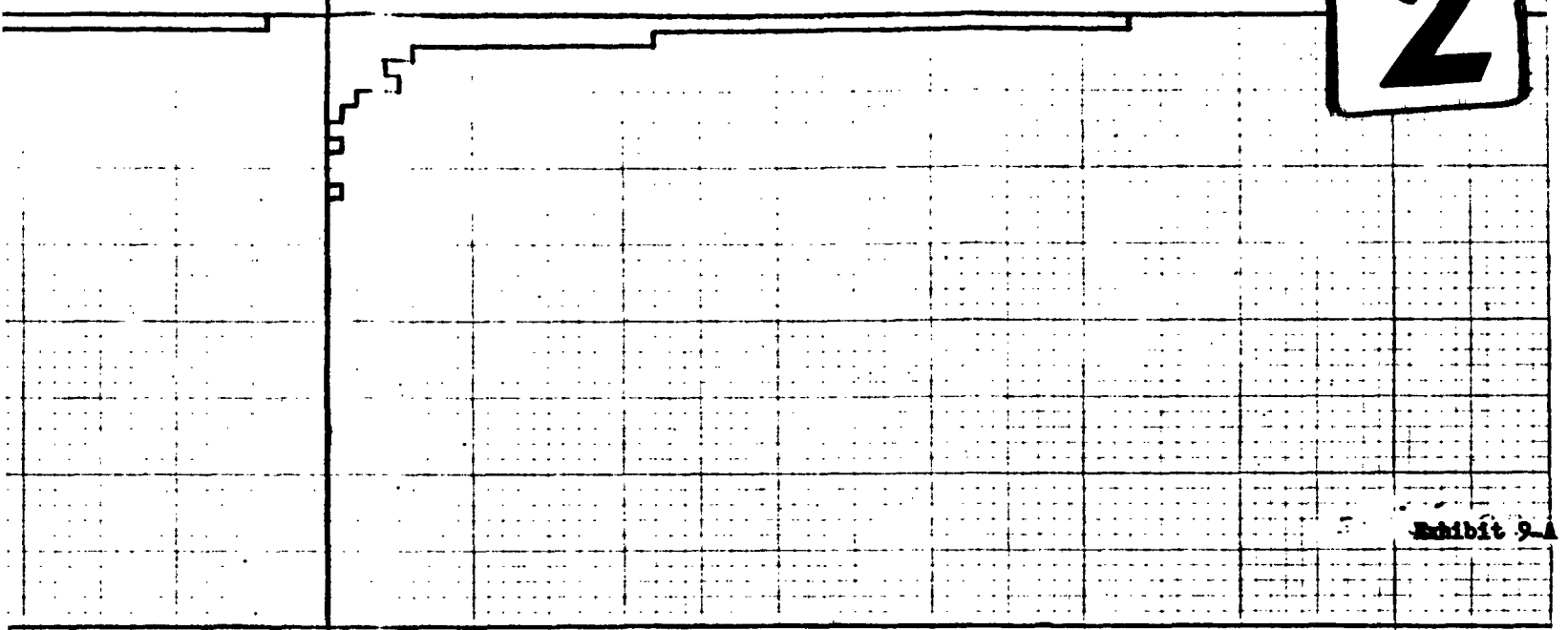


Exhibit 9-A

roups 10+15 @ 333hrs., 145°C Storage

Dry Oz @ 100°C

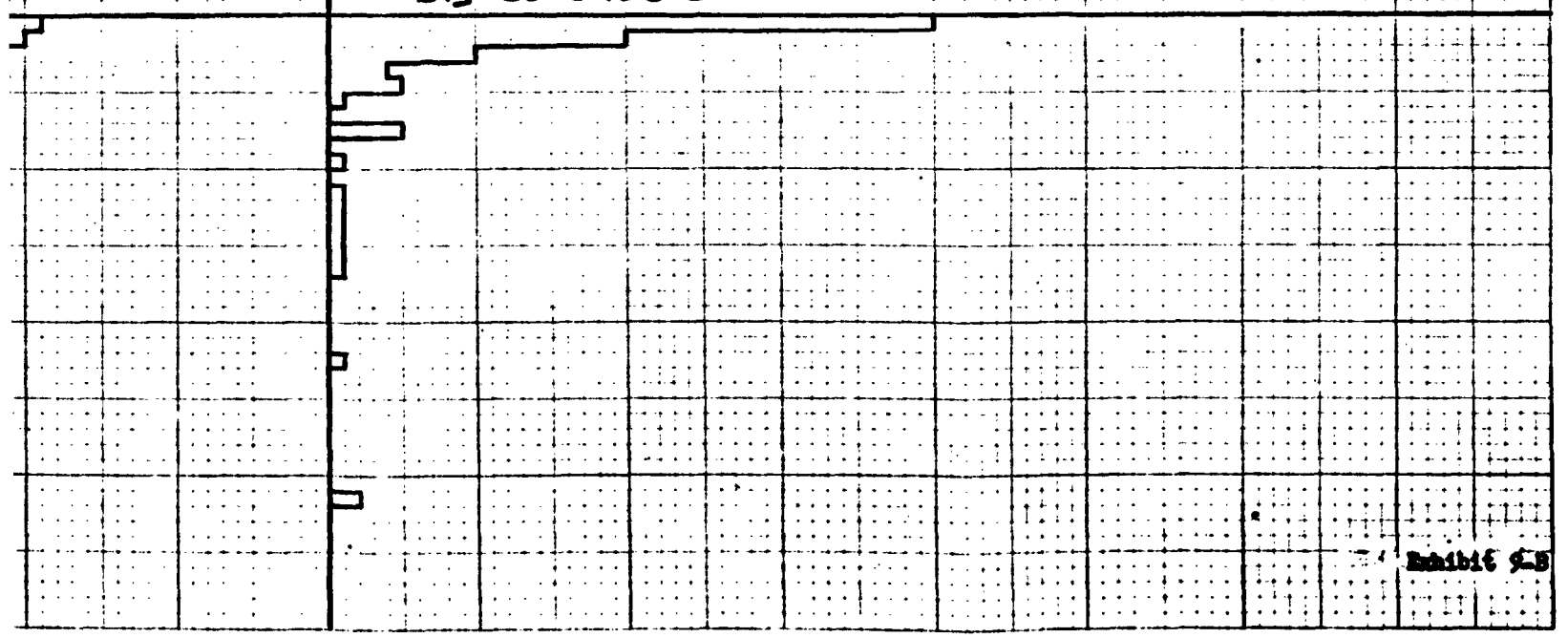


Exhibit 9-B

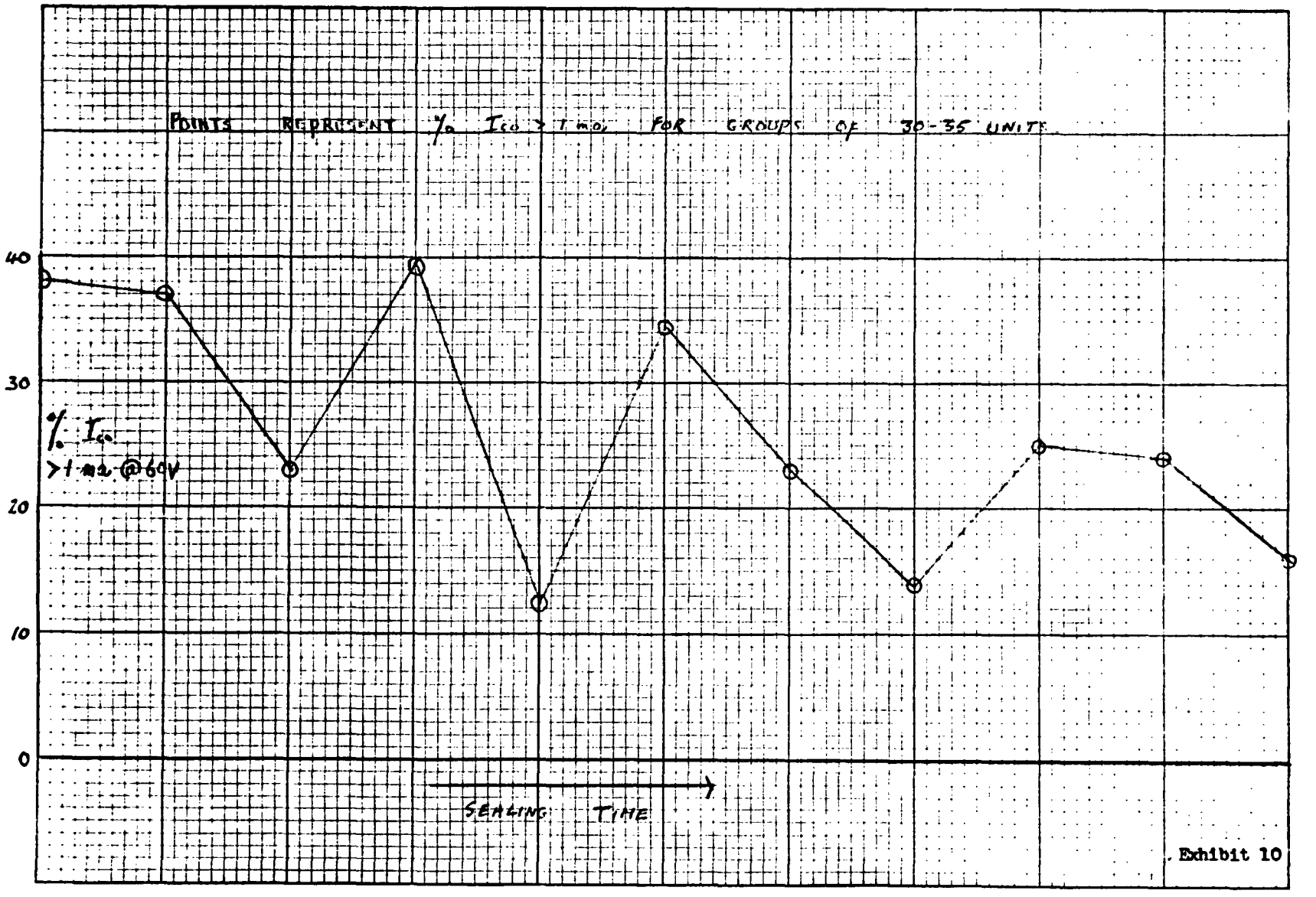
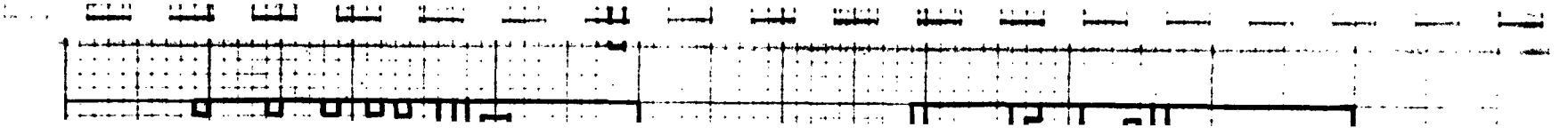
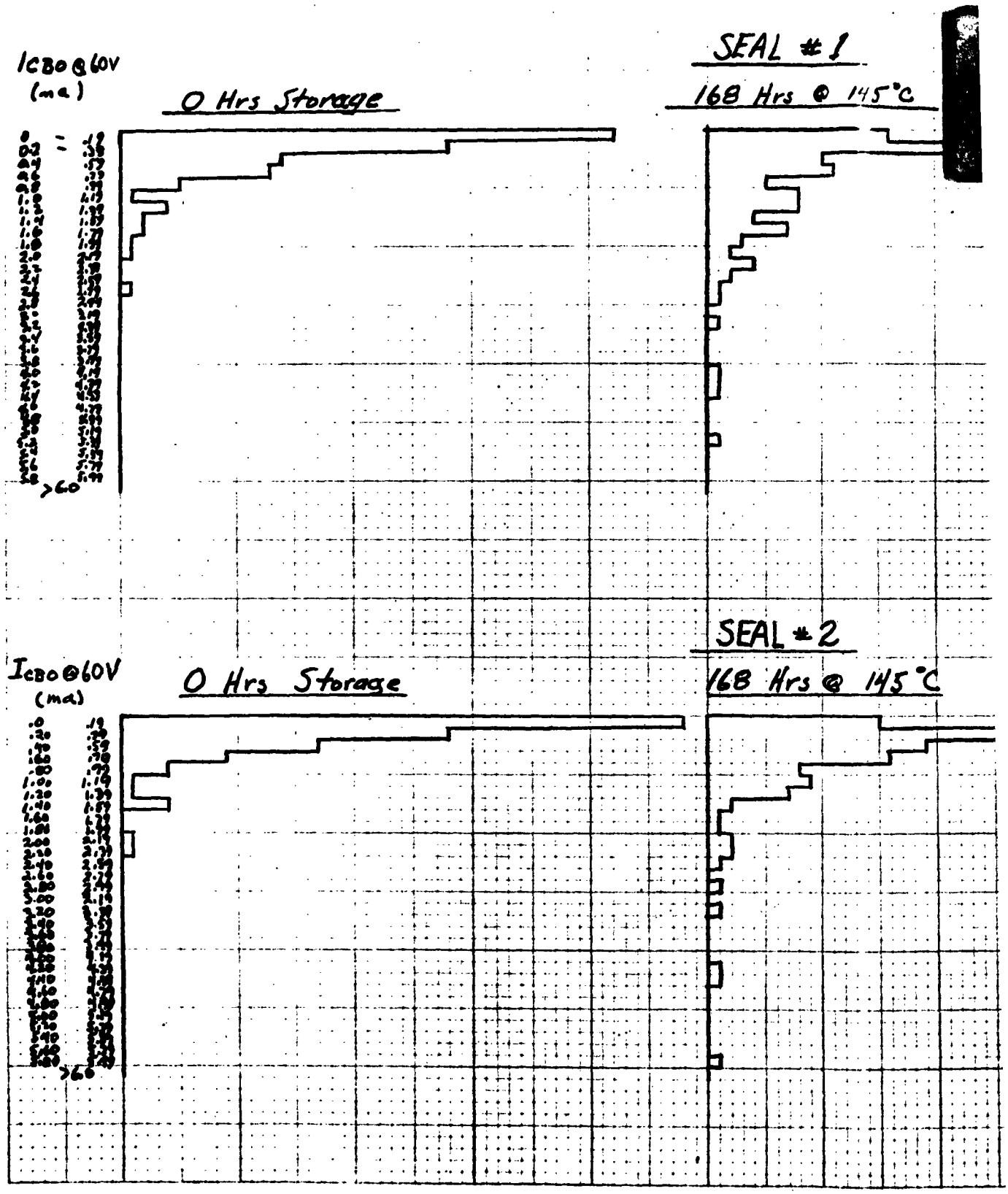


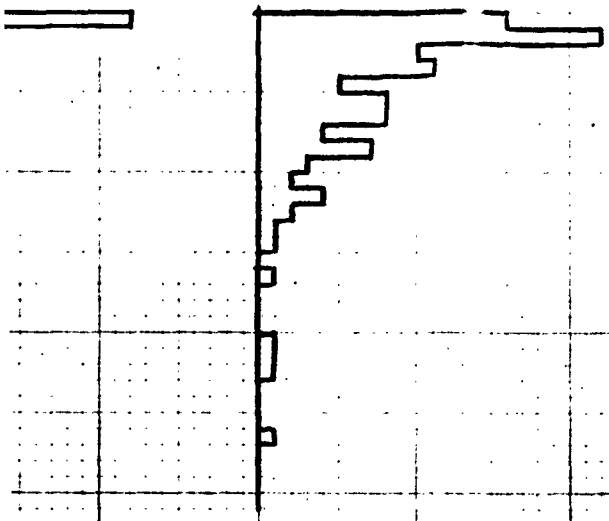
Exhibit 10



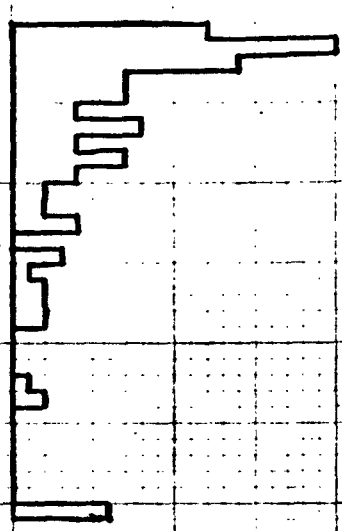

SEAL #1
I_{CBO} @ 60V (ma)
0 Hrs Storage
168 Hrs @ 145°C
>60
SEAL #2
I_{CBO} @ 60V (ma)
0 Hrs Storage
168 Hrs @ 145°C
>60

SEAL #1

168 Hrs @ 145°C



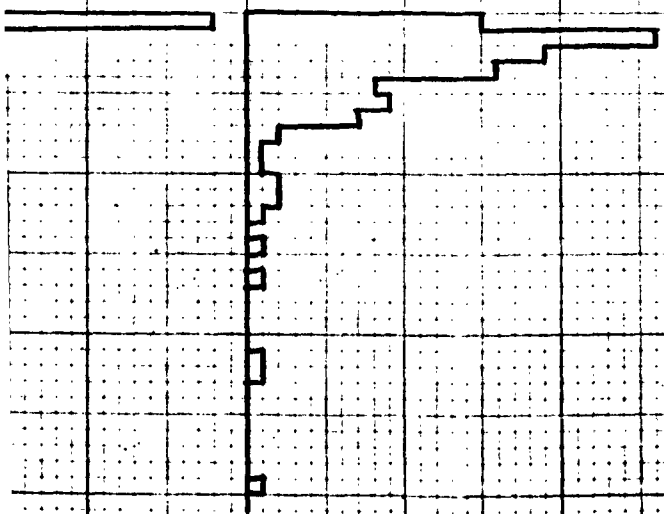
333 Hrs @ 145°C



2

SEAL #2

168 Hrs @ 145°C



333 Hrs @ 145°C

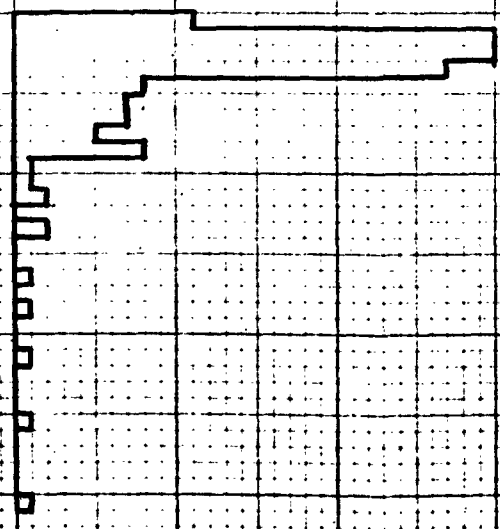
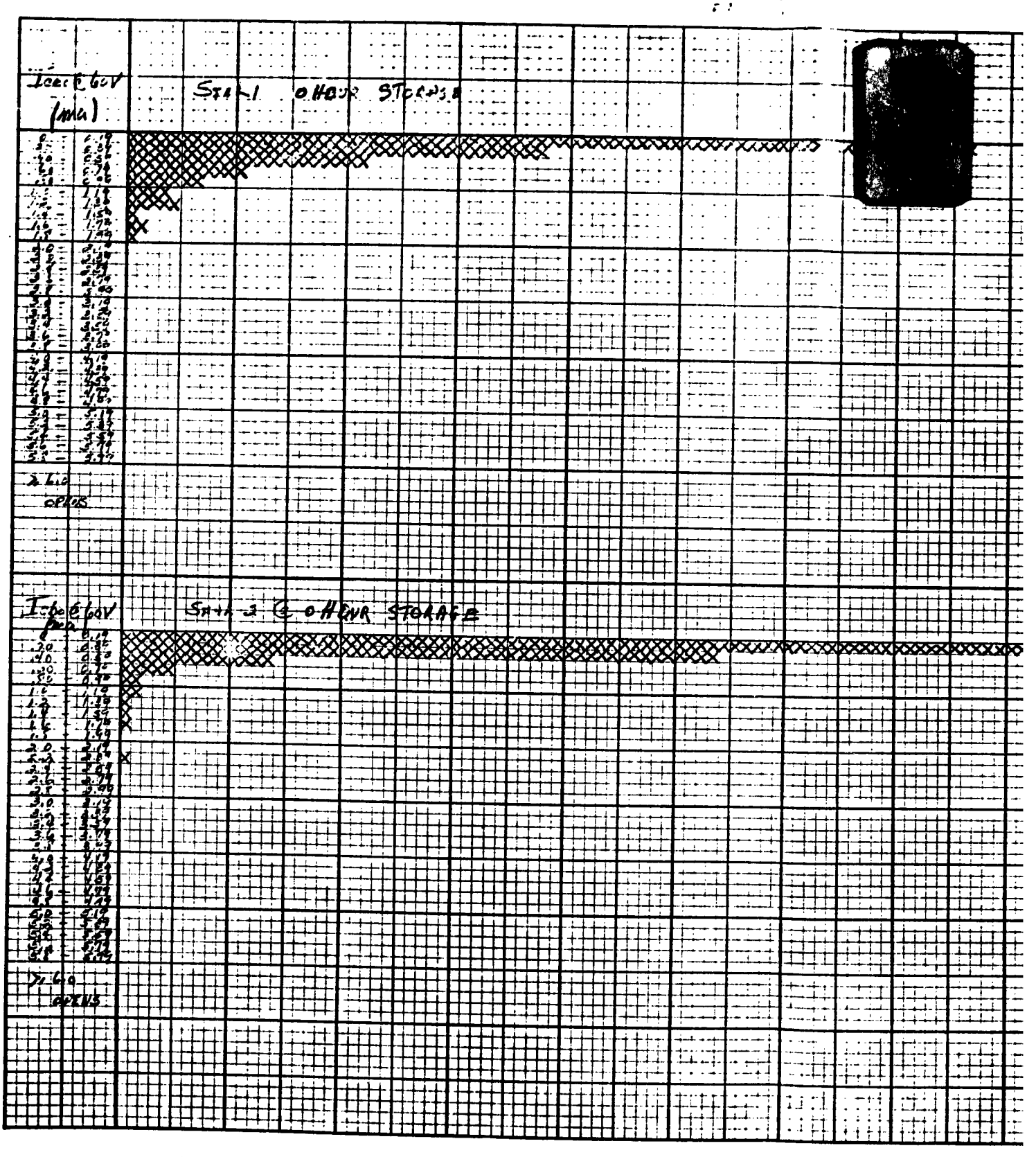
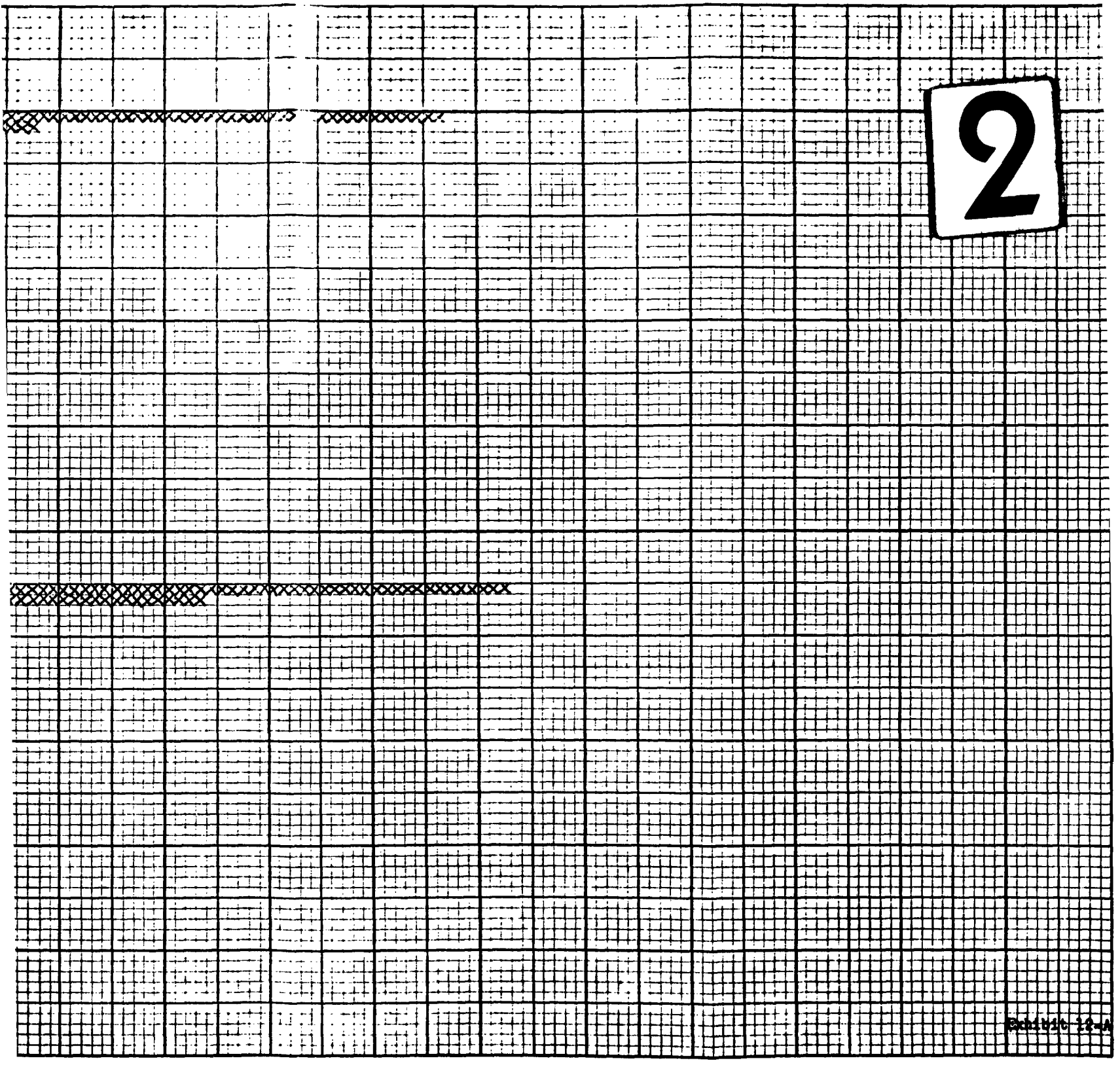
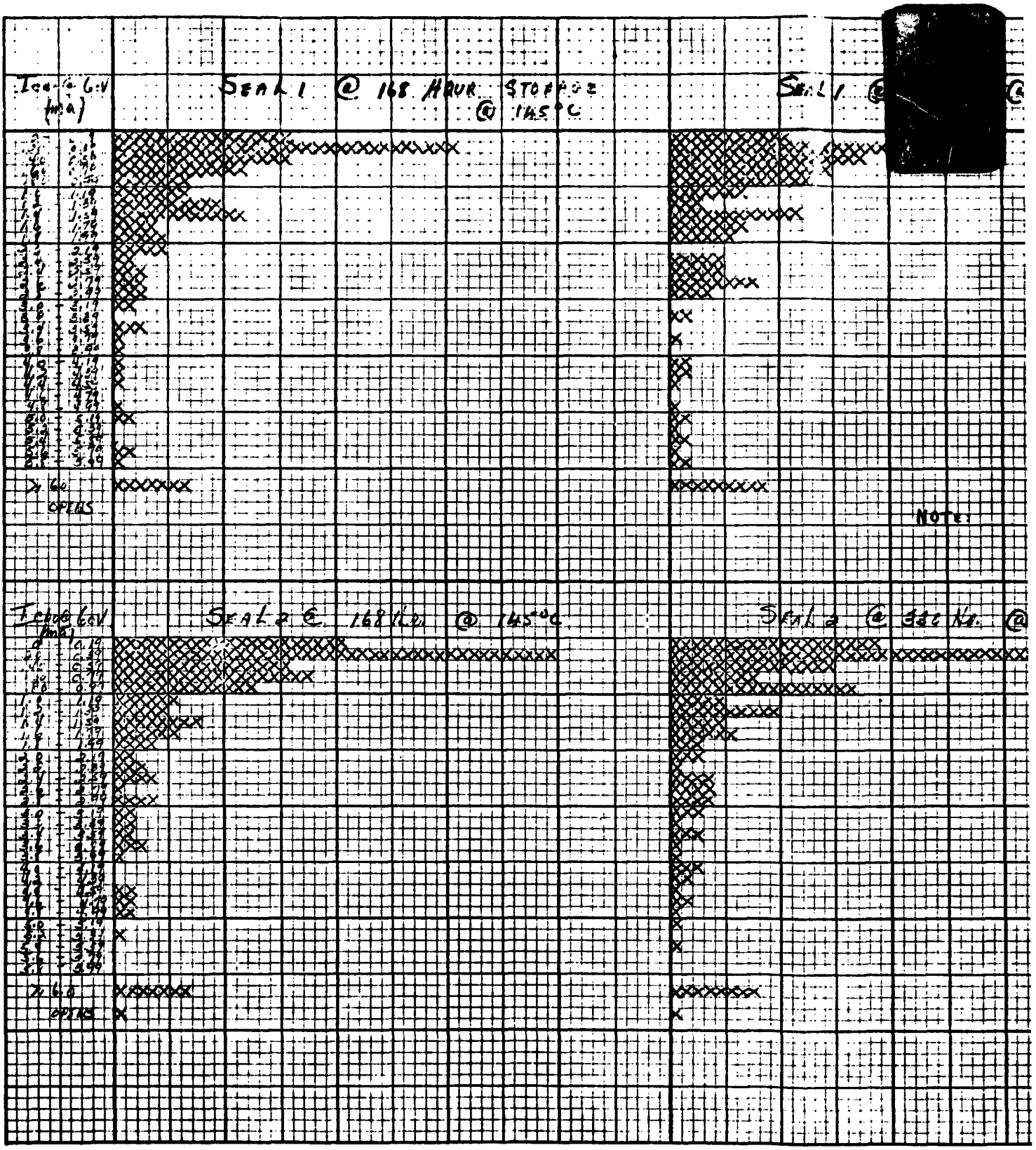
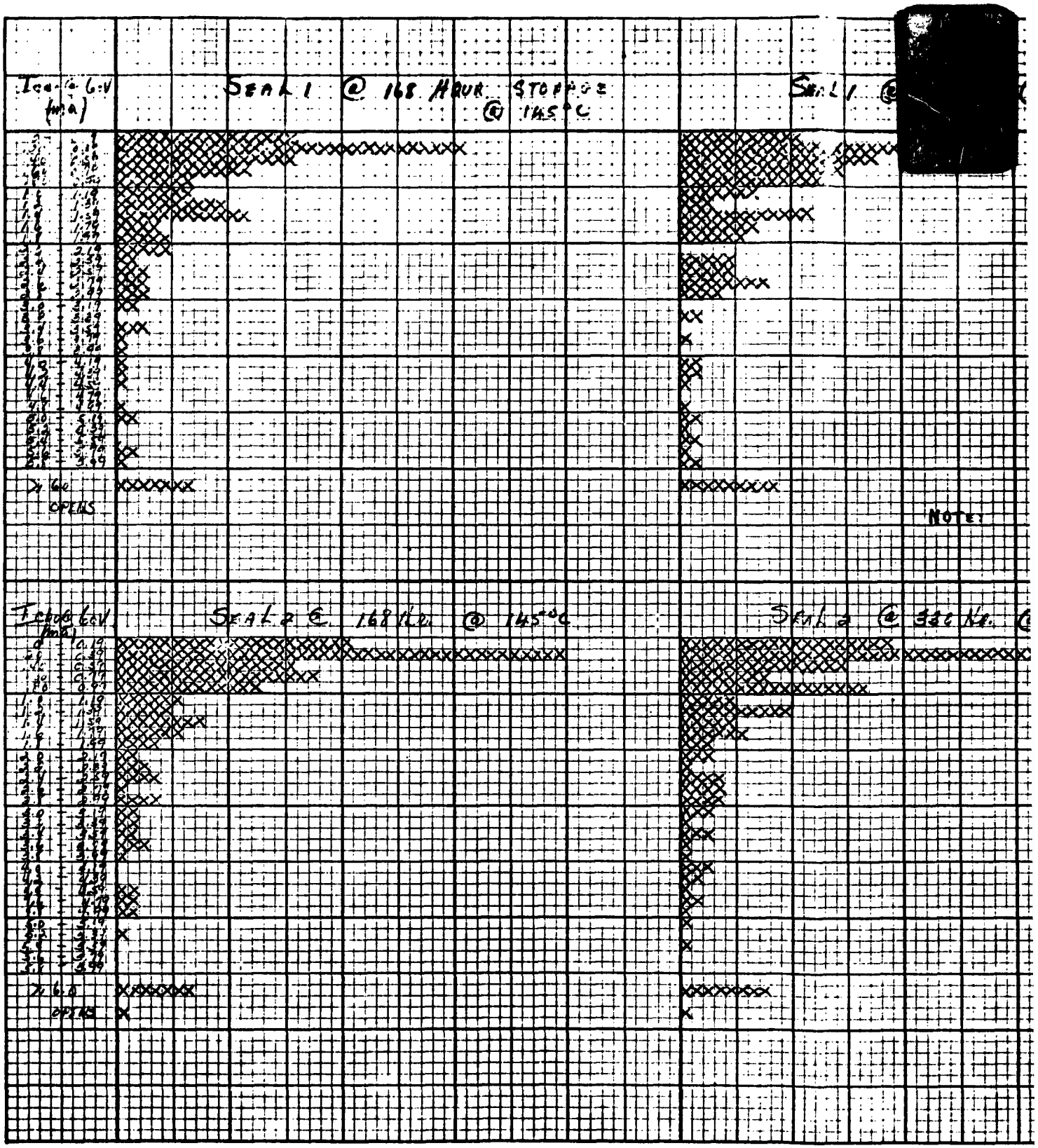


Exhibit 11




2
Exhibit 12-A





Seal 1 @ 330 HR. @ 145°C

2

NOTE: DURING STORAGE OF SEAL 1 AND SEAL 2 TEMPERATURE INCREASED TO 160°C FOR AN UNKNOWN TIME.

Seal 2 @ 330 Hr. @ 145°C

EXHIBIT 12-B

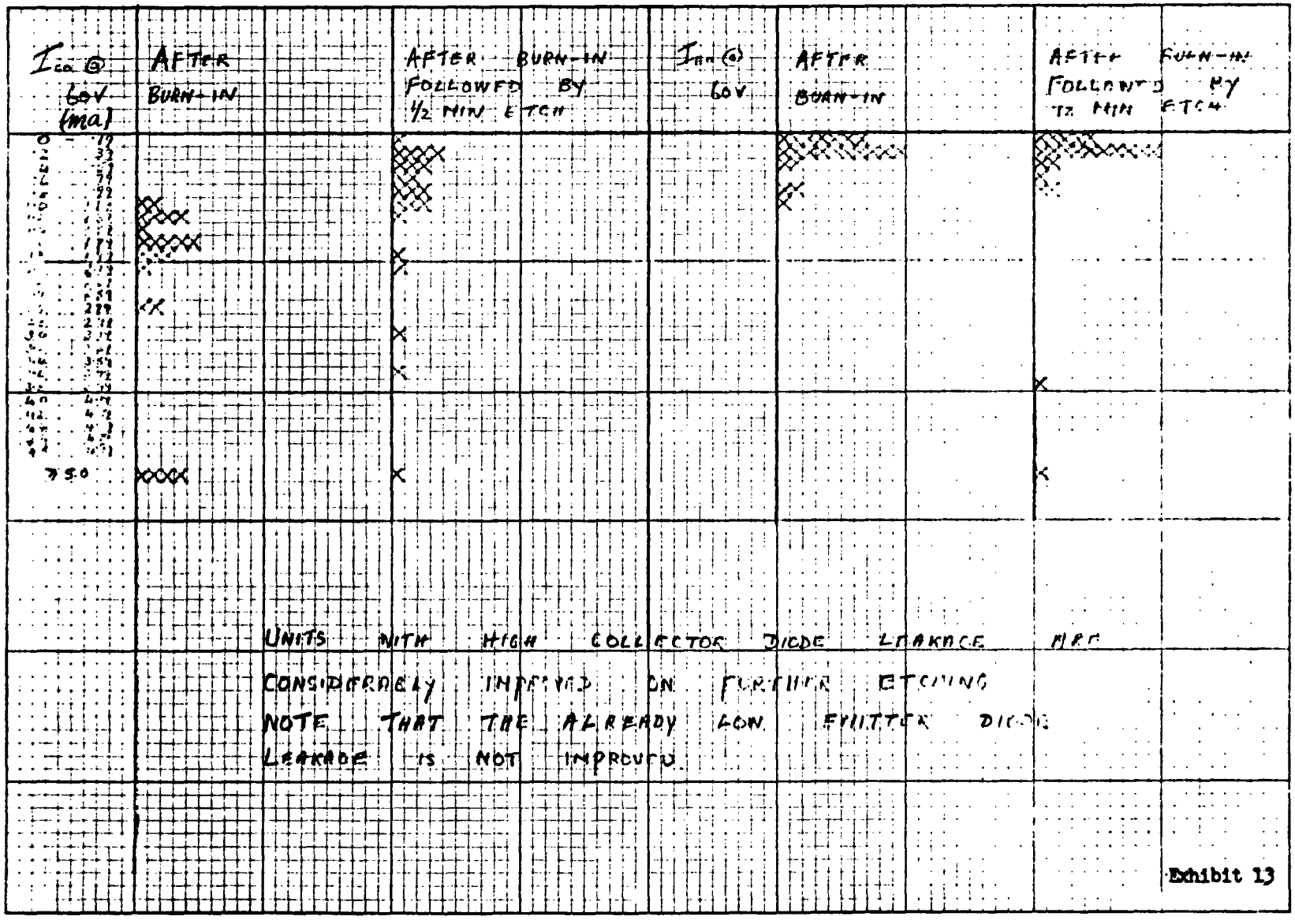

I_{CO} @ 60V (ma)
AFTER BURN-IN
AFTER BURN-IN FOLLOWED BY ½ MIN ETCH
I_{BO} @ 60V
AFTER BURN-IN
AFTER BURN-IN FOLLOWED BY ½ MIN ETCH
UNITS WITH HIGH COLLECTOR DIODE LEAKAGE MAY BE CONSIDERABLY IMPROVED ON FURTHER ETCHING
NOTE THAT THE ALREADY LOW EMITTER DIODE LEAKAGE IS NOT IMPROVED.

Exhibit 13

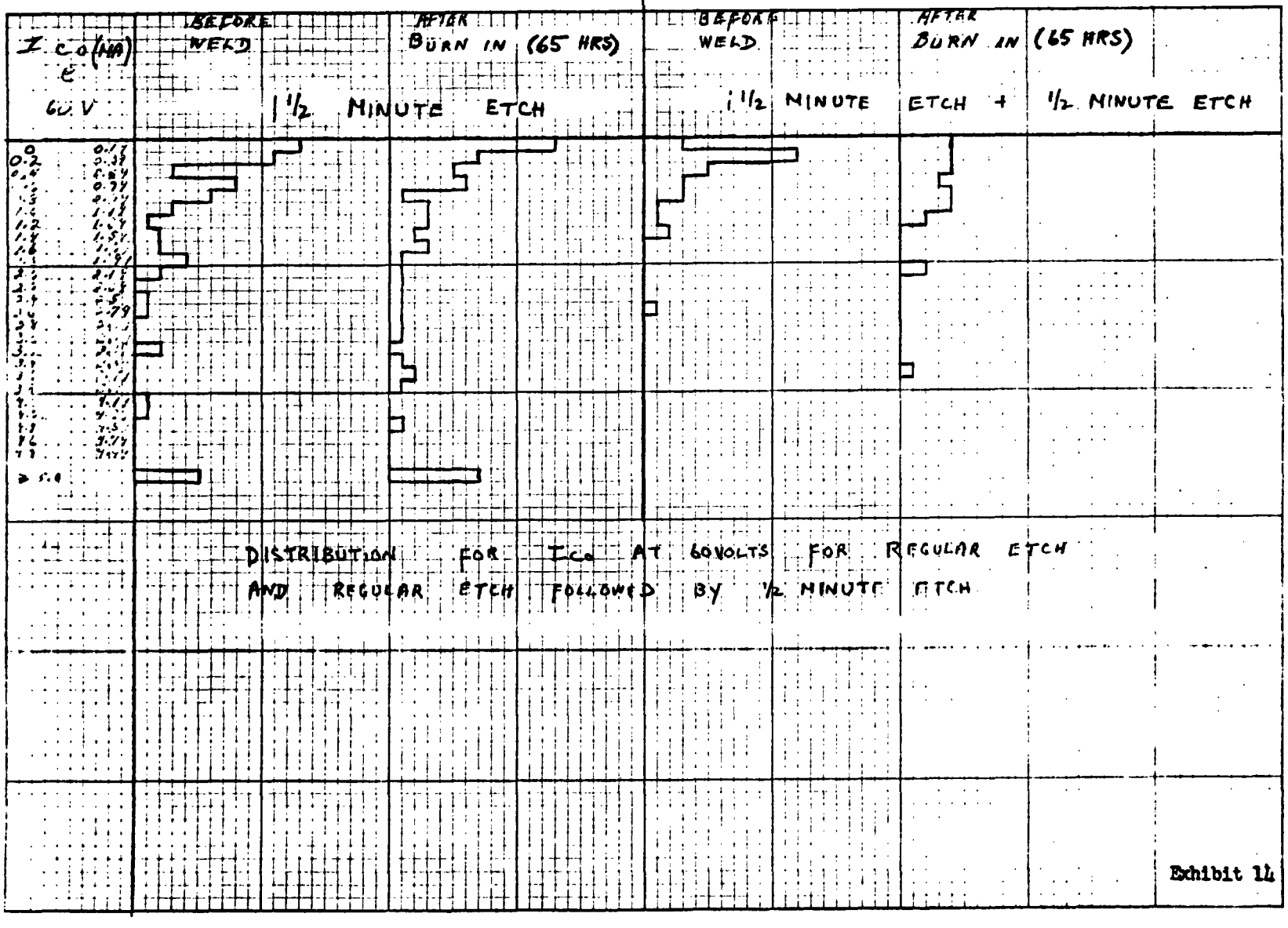

I_{Co} (μA) @ 60 V
BEFORE WELD
AFTER BURN IN (65 HRS)
1 1/2 MINUTE ETCH
BEFORE WELD
1 1/2 MINUTE ETCH
AFTER BURN IN (65 HRS)
ETCH + 1/2 MINUTE ETCH
DISTRIBUTION FOR I_{Co} AT 60 VOLTS FOR REGULAR ETCH AND REGULAR ETCH FOLLOWED BY 1/2 MINUTE ETCH

Exhibit 14

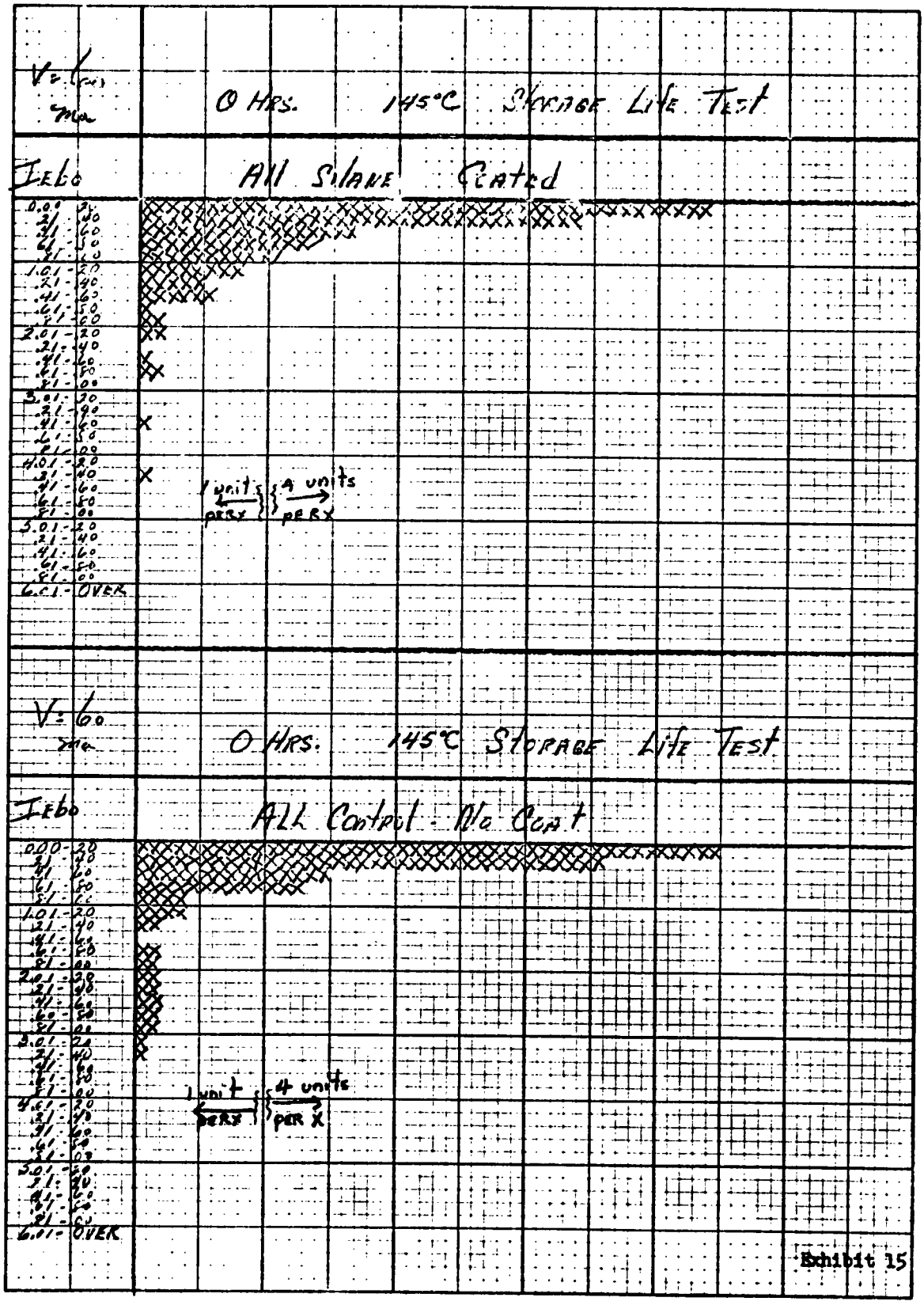

V = 60
0 HRS. 145°C Storage Life Test
All Silane Coated
0.00 - 20
.21 - 40
.41 - 60
.61 - 80
.81 - 1.00
1.01 - 20
.21 - 40
.41 - 60
.61 - 80
.81 - 2.00
2.01 - 20
.21 - 40
.41 - 60
.61 - 80
.81 - 3.00
3.01 - 20
.21 - 40
.41 - 60
.61 - 80
.81 - 4.00
4.01 - 20
.21 - 40
.41 - 60
.61 - 80
.81 - 5.00
5.01 - 20
.21 - 40
.41 - 60
.61 - 80
.81 - 6.00
6.01 - OVER
1 unit per X
4 units per X
V = 60
0 HRS. 145°C Storage Life Test
All Control - No Coat
0.00 - 20
.21 - 40
.41 - 60
.61 - 80
.81 - 1.00
1.01 - 20
.21 - 40
.41 - 60
.61 - 80
.81 - 2.00
2.01 - 20
.21 - 40
.41 - 60
.61 - 80
.81 - 3.00
3.01 - 20
.21 - 40
.41 - 60
.61 - 80
.81 - 4.00
4.01 - 20
.21 - 40
.41 - 60
.61 - 80
.81 - 5.00
5.01 - 20
.21 - 40
.41 - 60
.61 - 80
.81 - 6.00
6.01 - OVER
1 unit per X
4 units per X

Exhibit 15

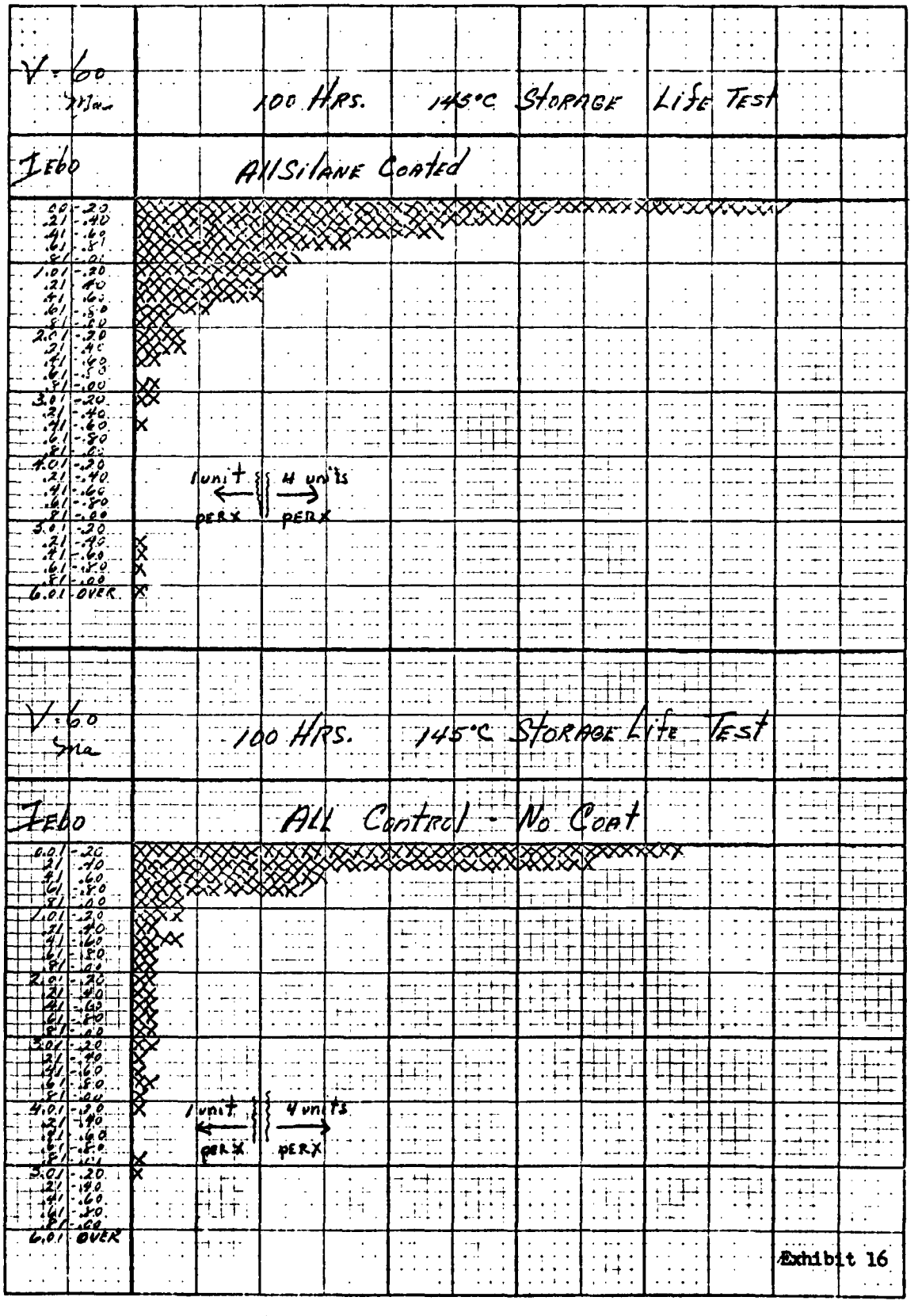


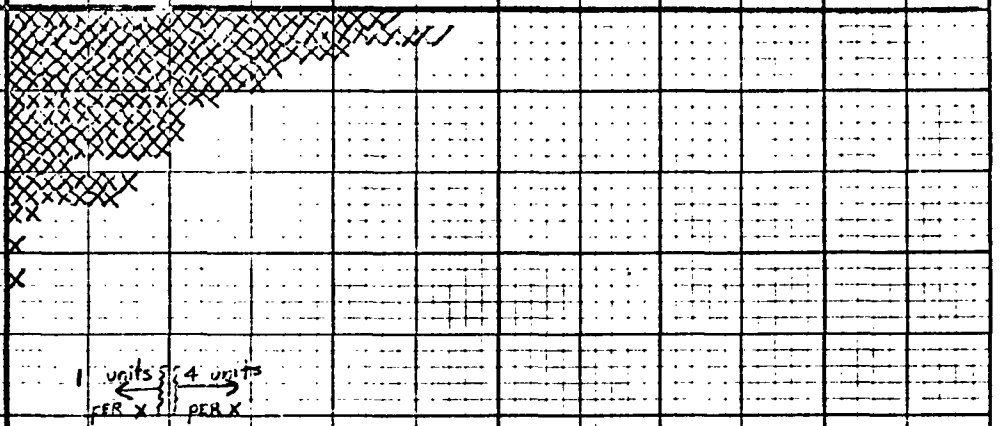
Exhibit 16

V: 60
Ina

0 HRS. 145°C STORAGE LIFE TEST

Icbo

All Silane Coated



V: 60
Ina

0 HRS. 145°C STORAGE LIFE TEST

Icbo

All Control - No Coat

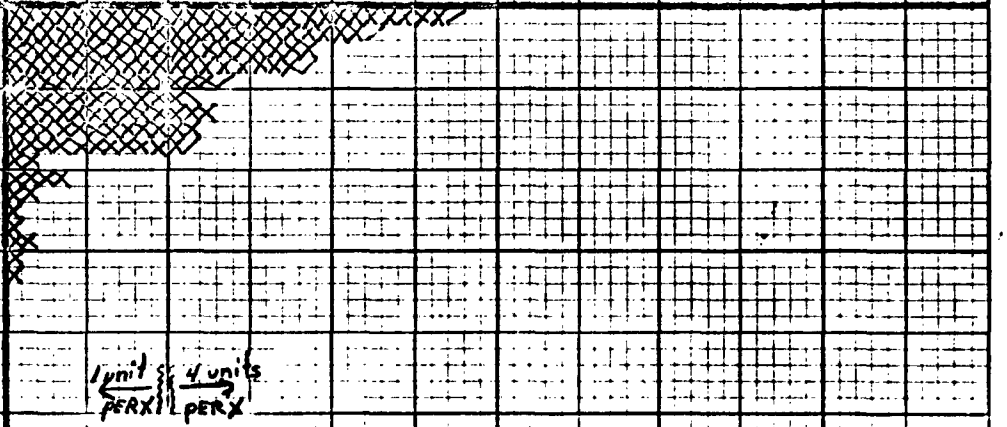


Exhibit 17

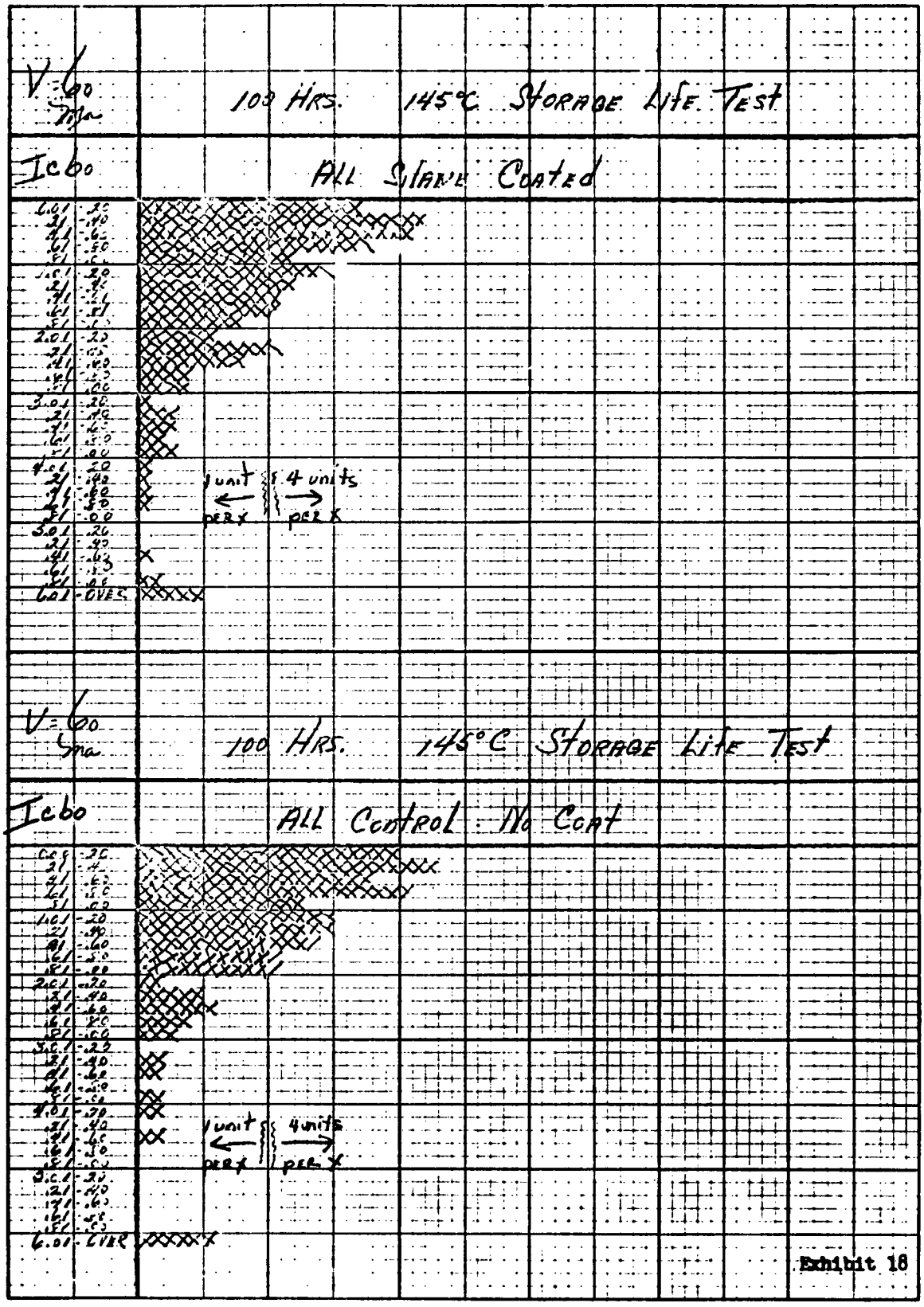


Exhibit 18

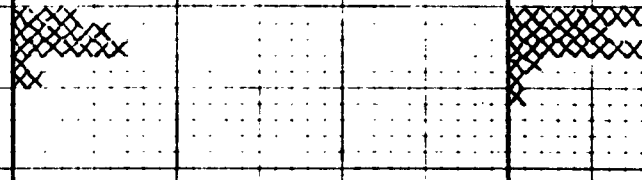
Ic = 2a
Vcb = 2V
2N2

LOT E 145°C STORAGE LIFE TEST

Ib

0 HRS. COATED

0 HRS. CONTROL



LOT E 145°C STORAGE LIFE TEST

Ib

344 HRS. COATED

344 HRS. CONTROL

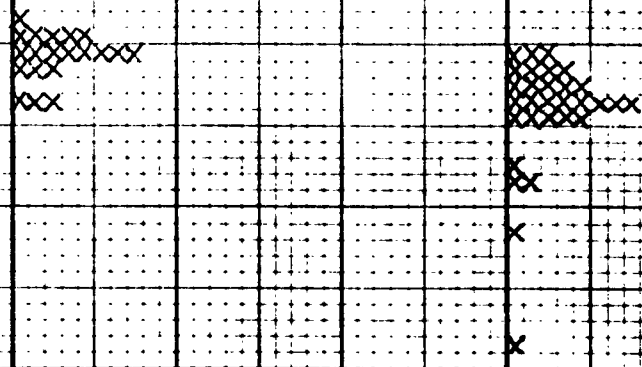


Exhibit 19

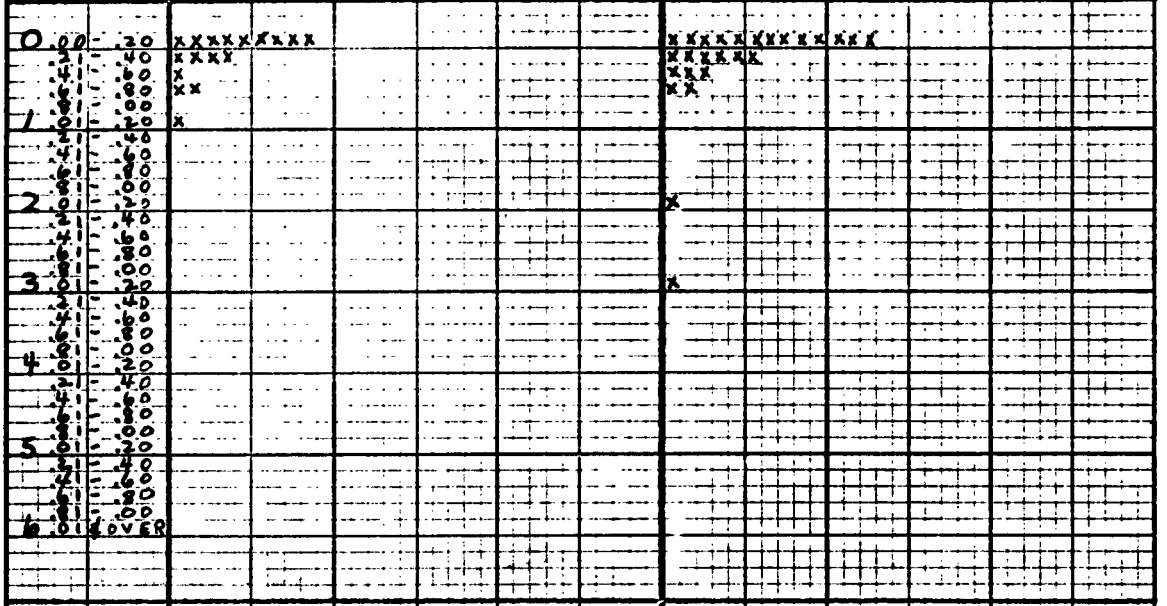
V = 60 ma

Lot F 1-20 0 hrs., 145°C Storage Life Test

IEBO

Silicate Coated

Control (no coat)



ICBO

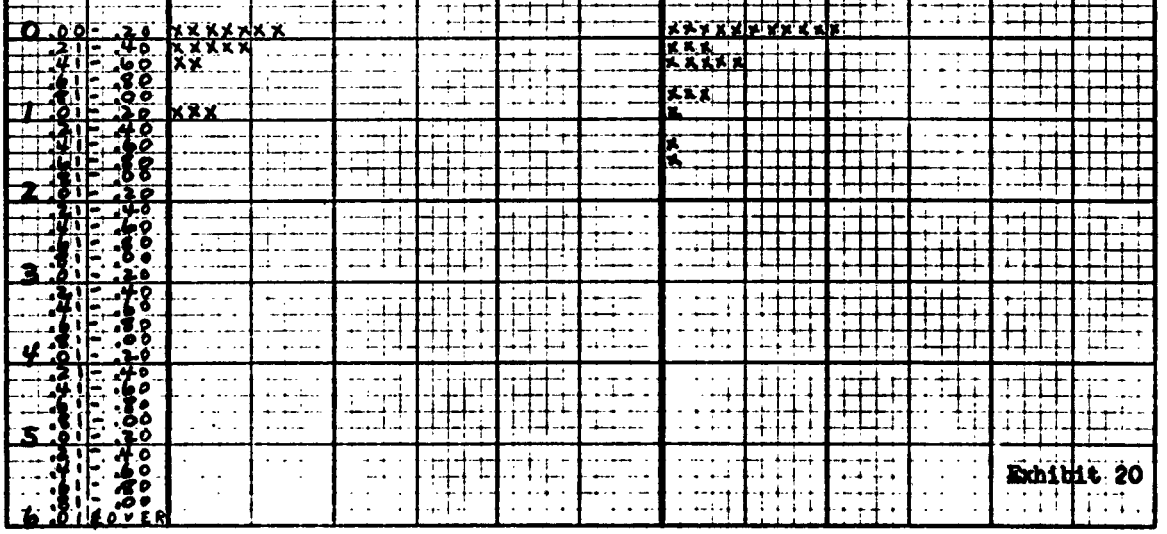
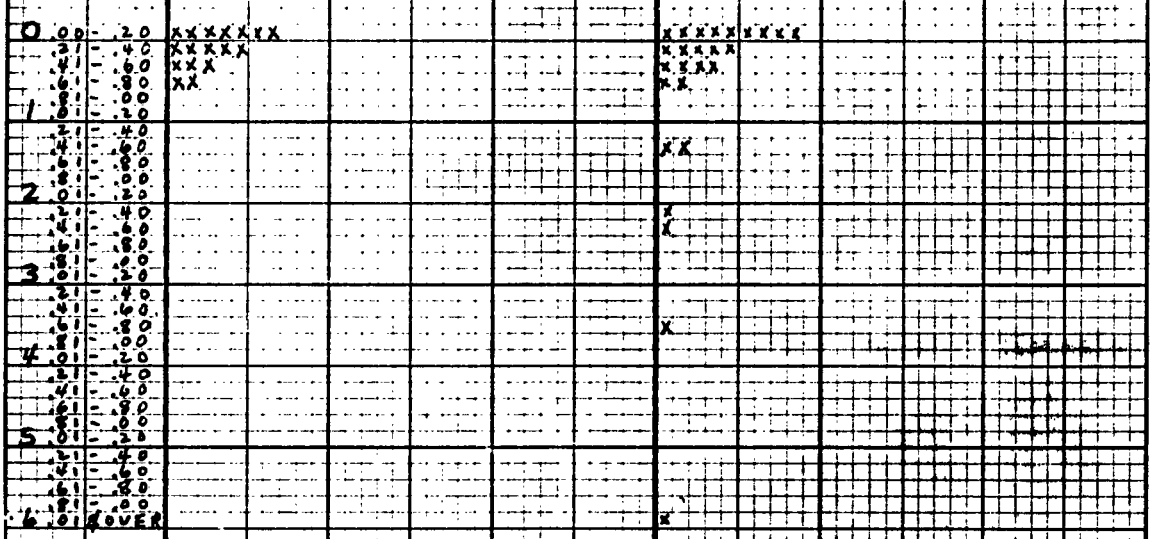


Exhibit 20

V=60

ma Lot F 1+20 After 344 hrs. 145°C Storage Life Test

IEBO Silicate Coated Control (no coat)



ICBO

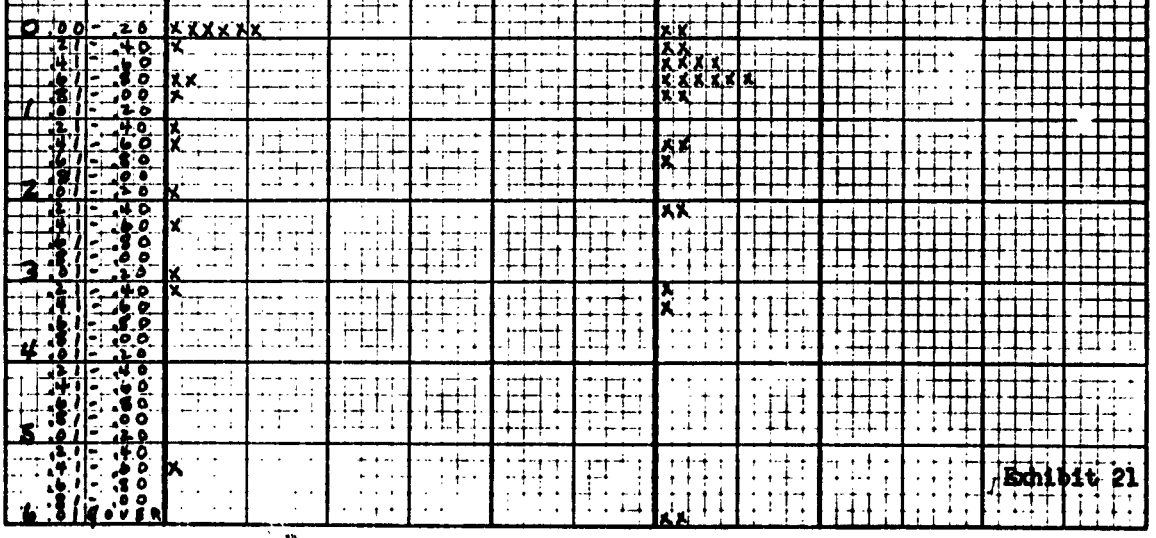
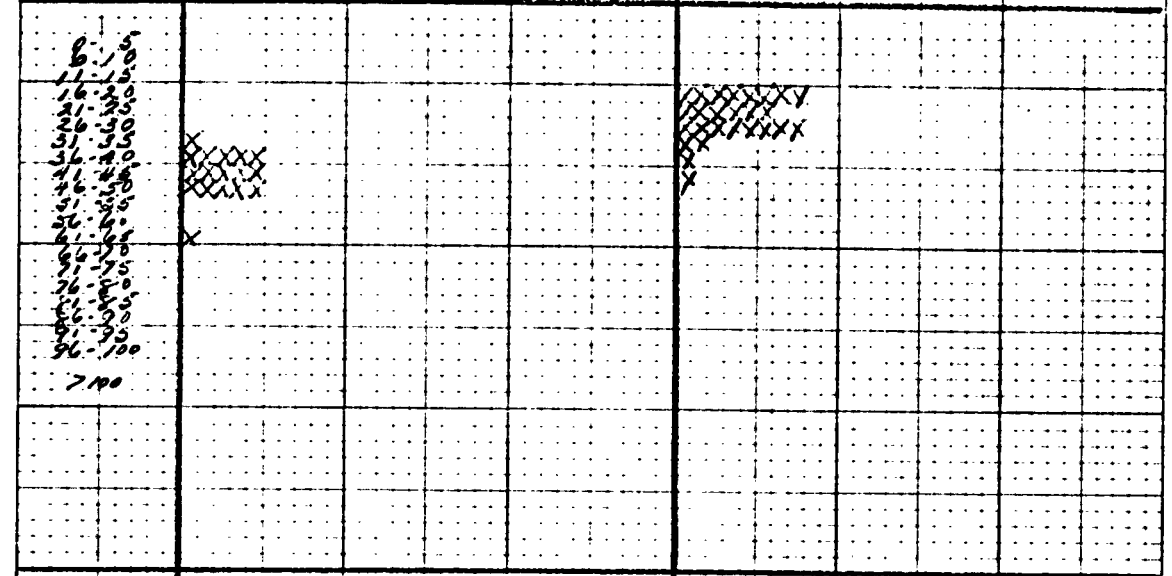


Exhibit 21

Ic - 2A
Ycb - 2V
mid

Lot F 1:20 Silicate — 145°C Storage Life Test

Ib — 0 Hrs Coated — 0 Hrs Control



Lot F 1:20 Silicate — 145°C Storage Life Test

Ib — 344 Hrs Coated — 344 Hrs. Control

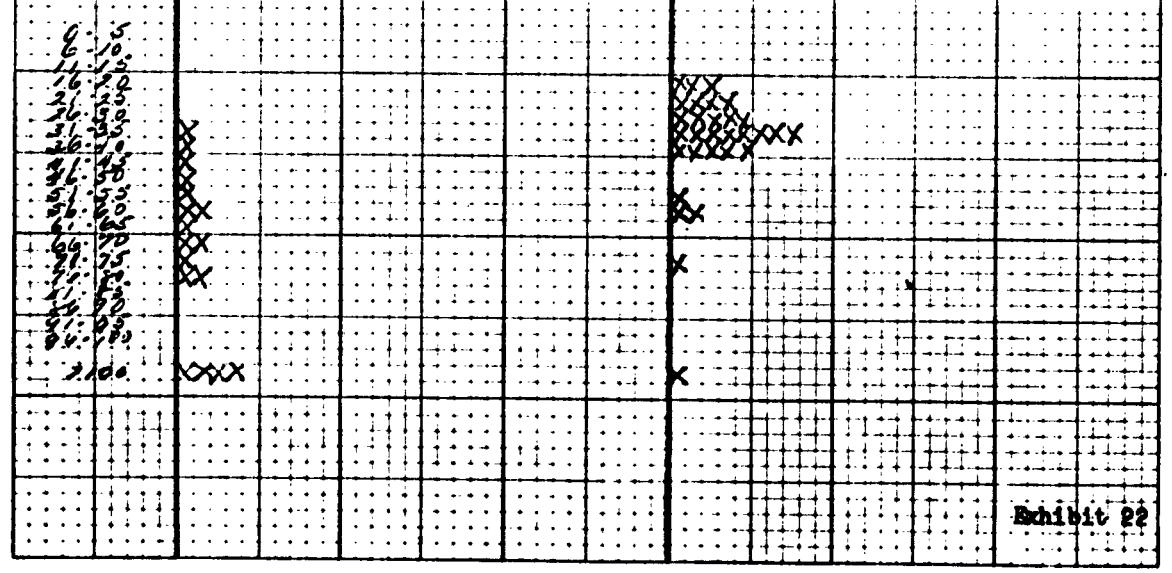


Exhibit 22

EUGENE DIETZGEN CO
MADE IN U. S. A.

NO 340 -10 DIETZGEN GRAPH PAPER
10 X 10 PER INCH

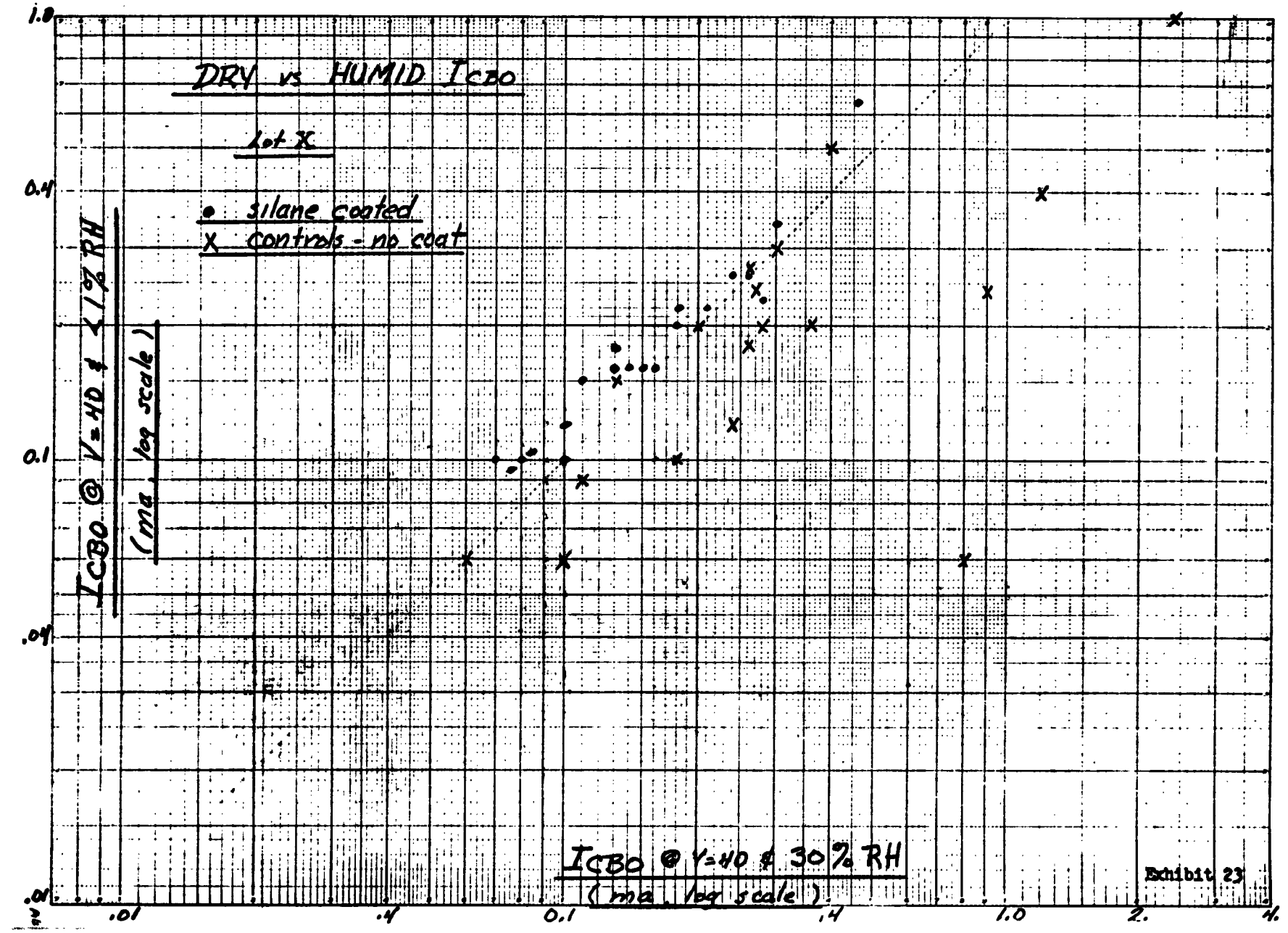
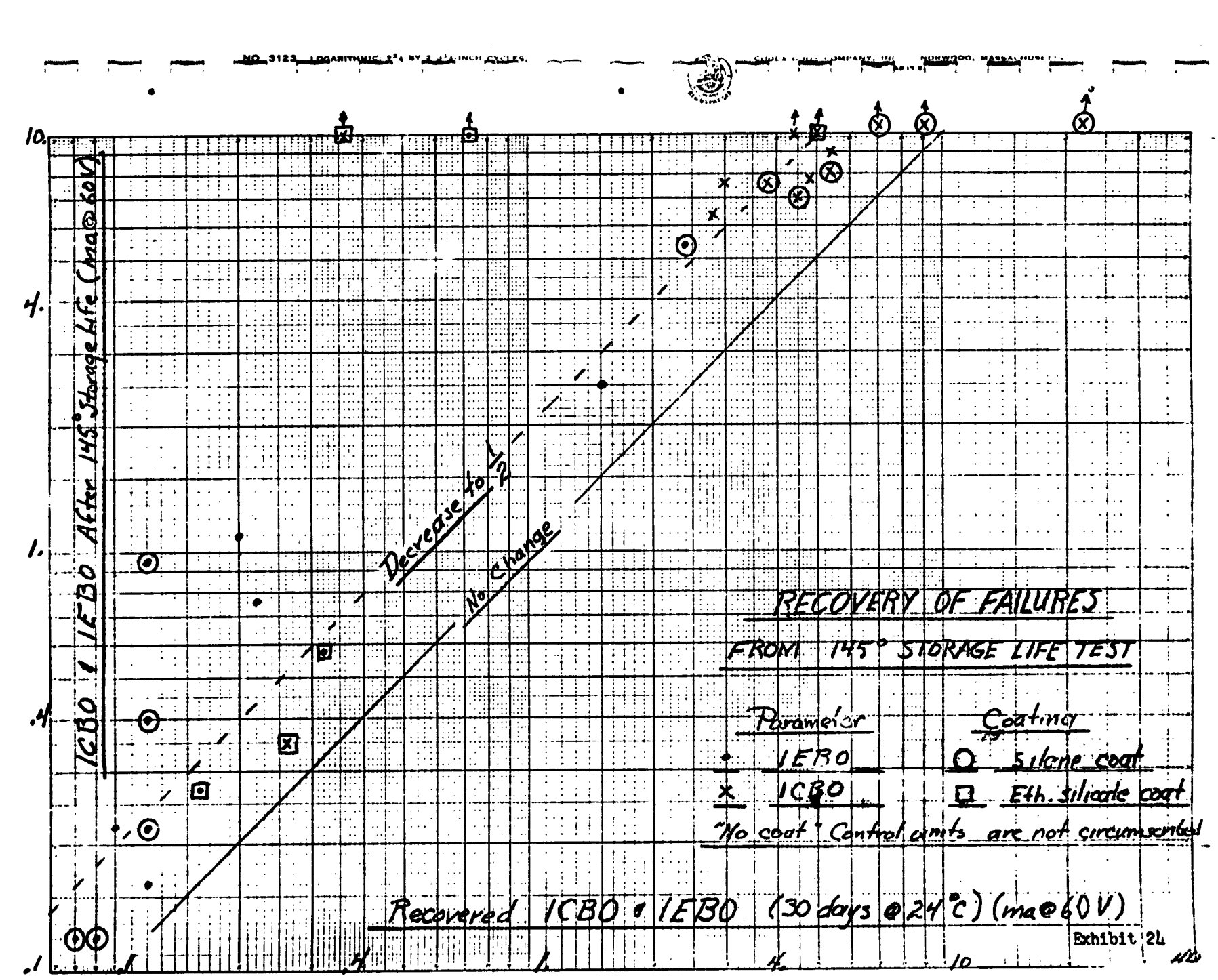
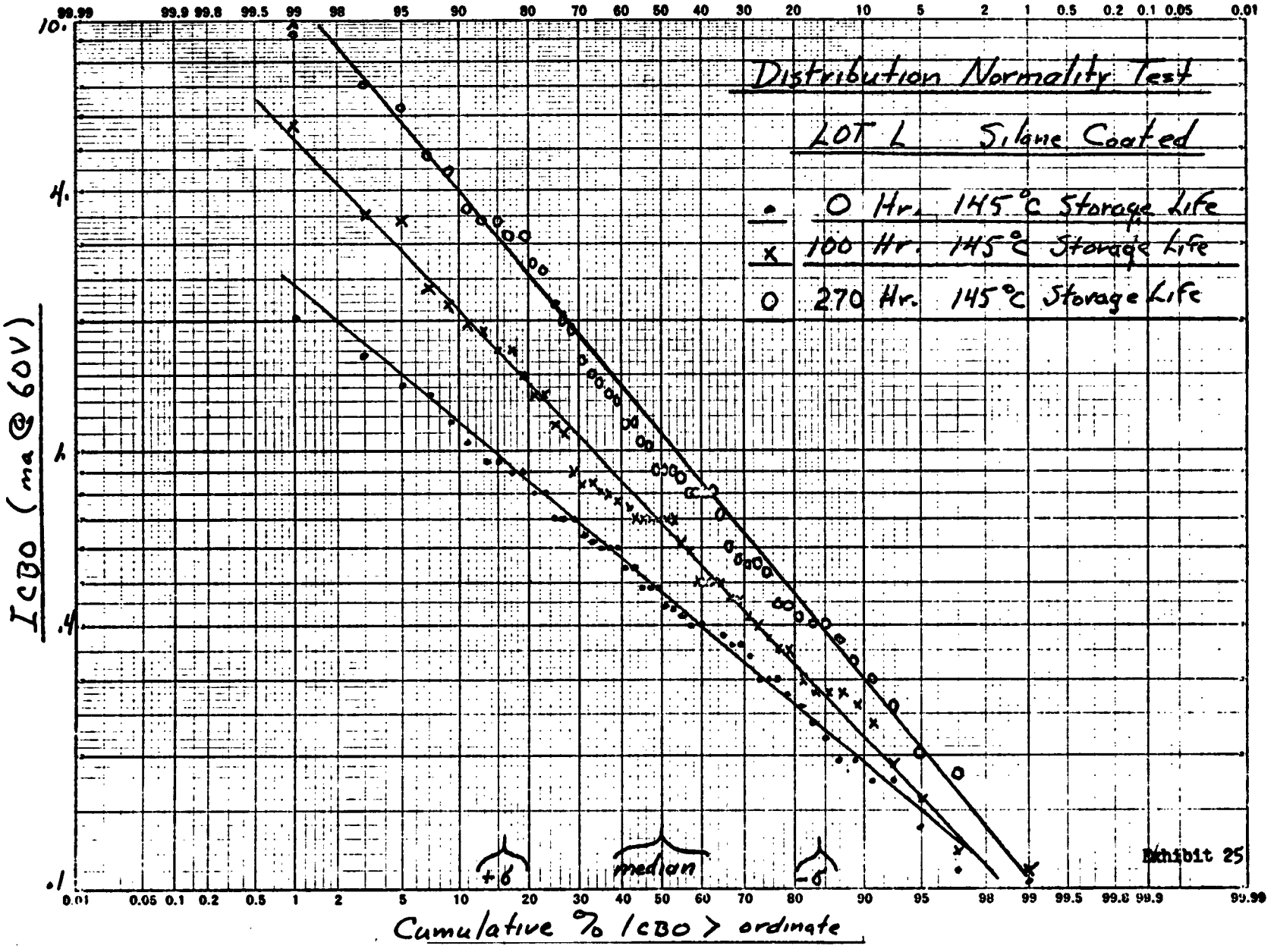


Exhibit 23


ICBO & IEBO After 145° Storage Life (ma@60V)
10.
4.
1.
.4
.1
Decrease to 1/2
No Change
RECOVERY OF FAILURES
FROM 145° STORAGE LIFE TEST
Parameter
IEBO
ICBO
Coating
Silane coat
Eth. silicate coat
"No coat" Control units are not circumscribed
Recovered ICBO & IEBO (30 days @ 24°C) (ma@60V)
Exhibit 24



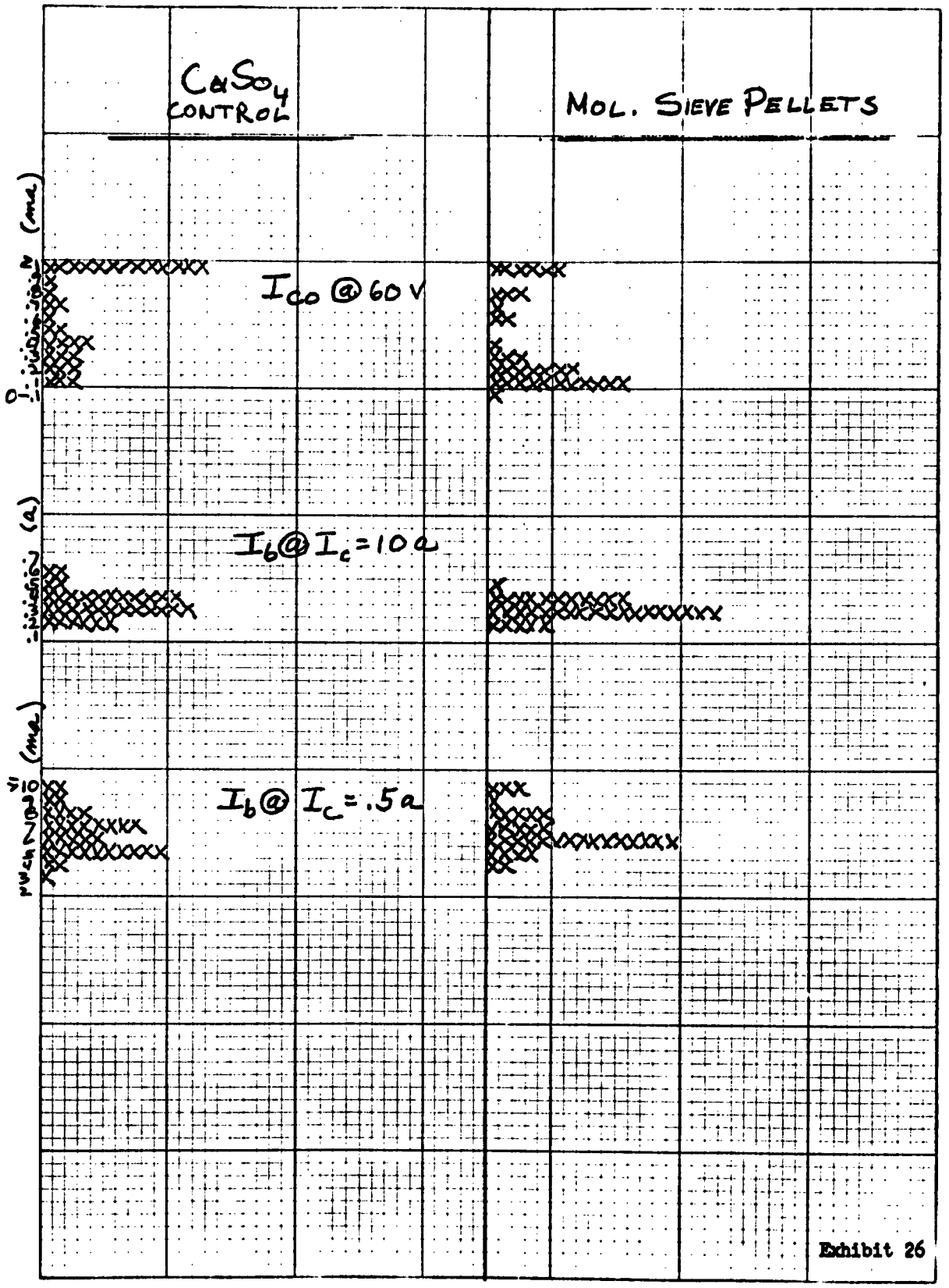
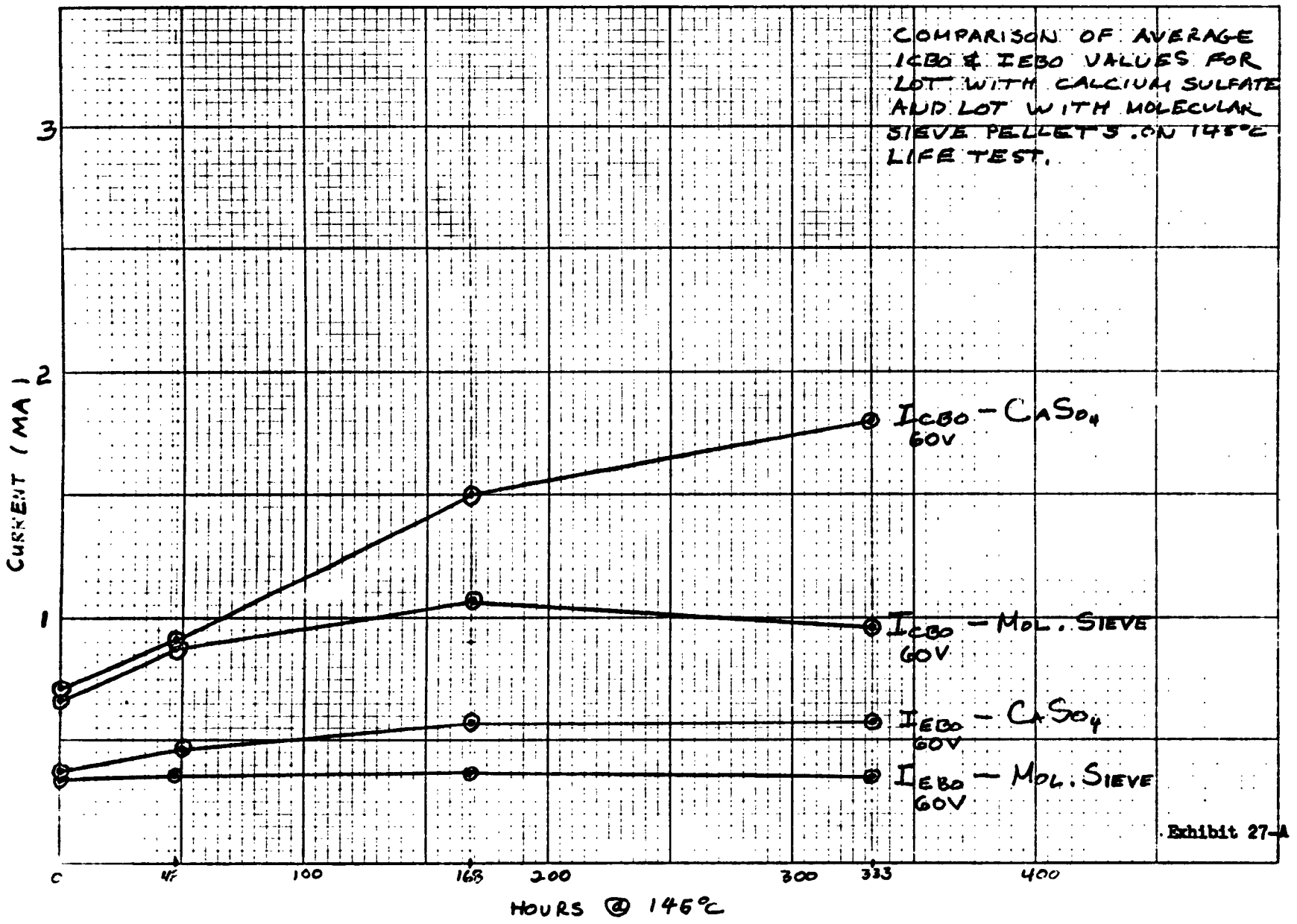
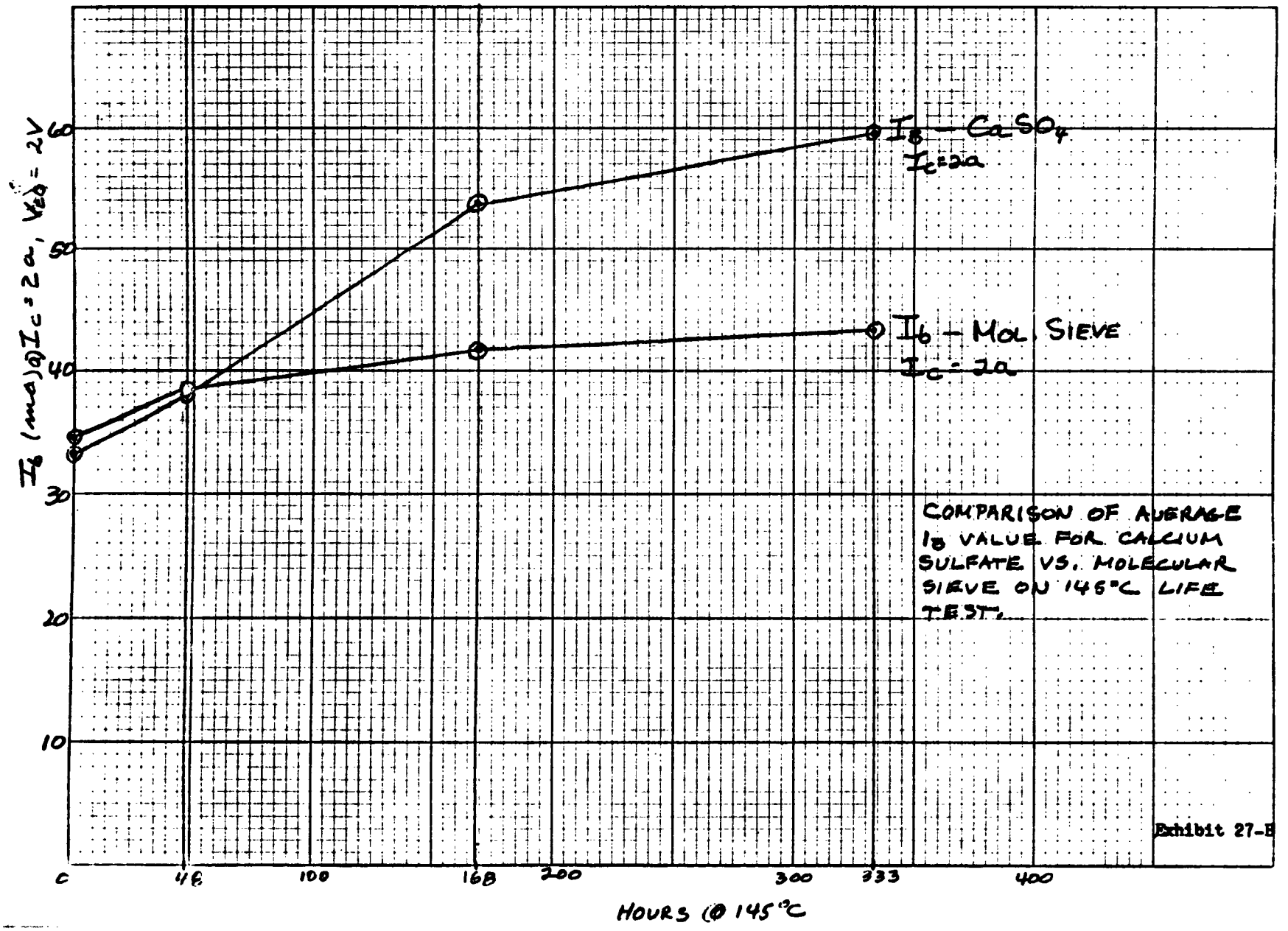
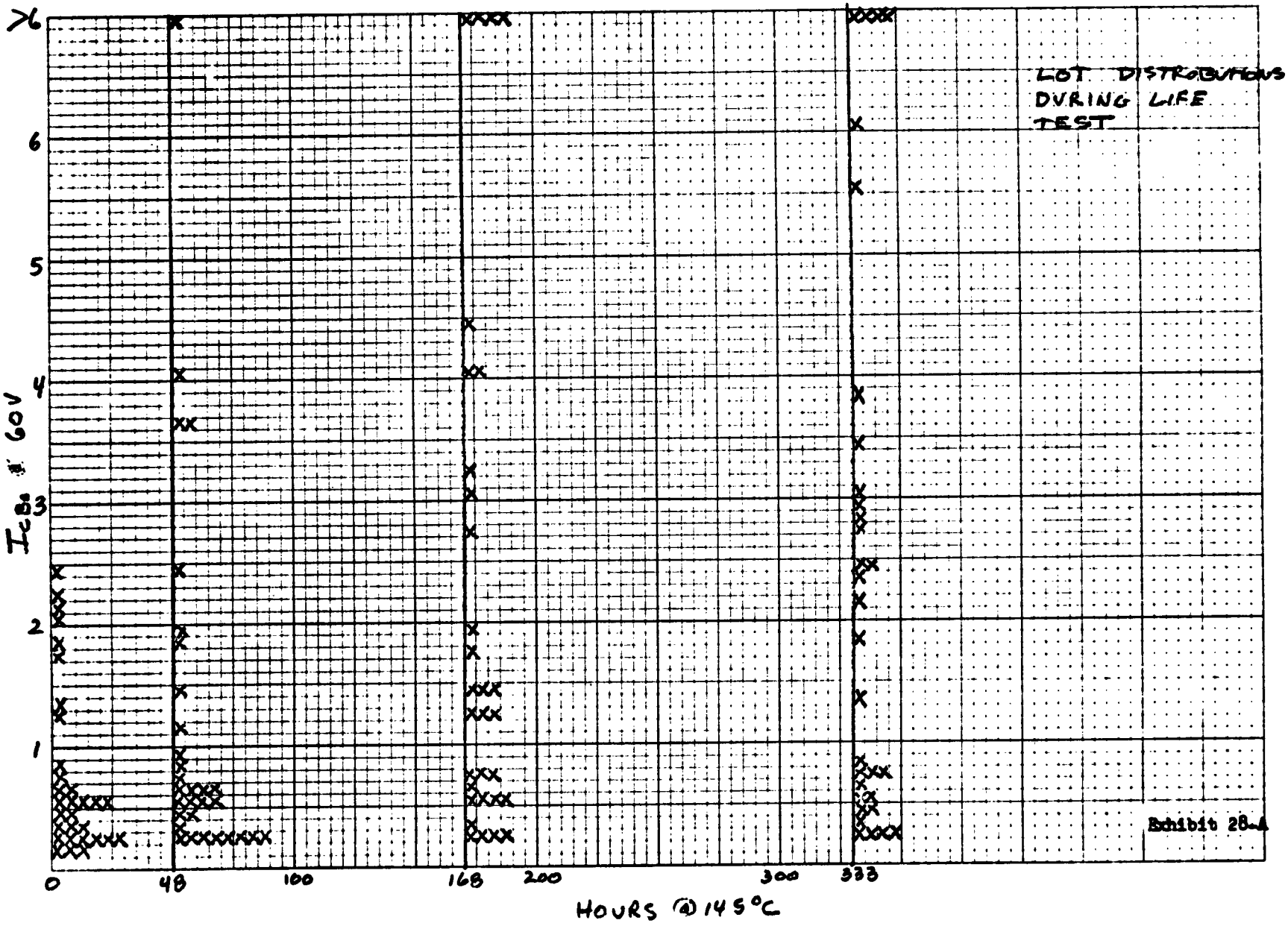


Exhibit 26

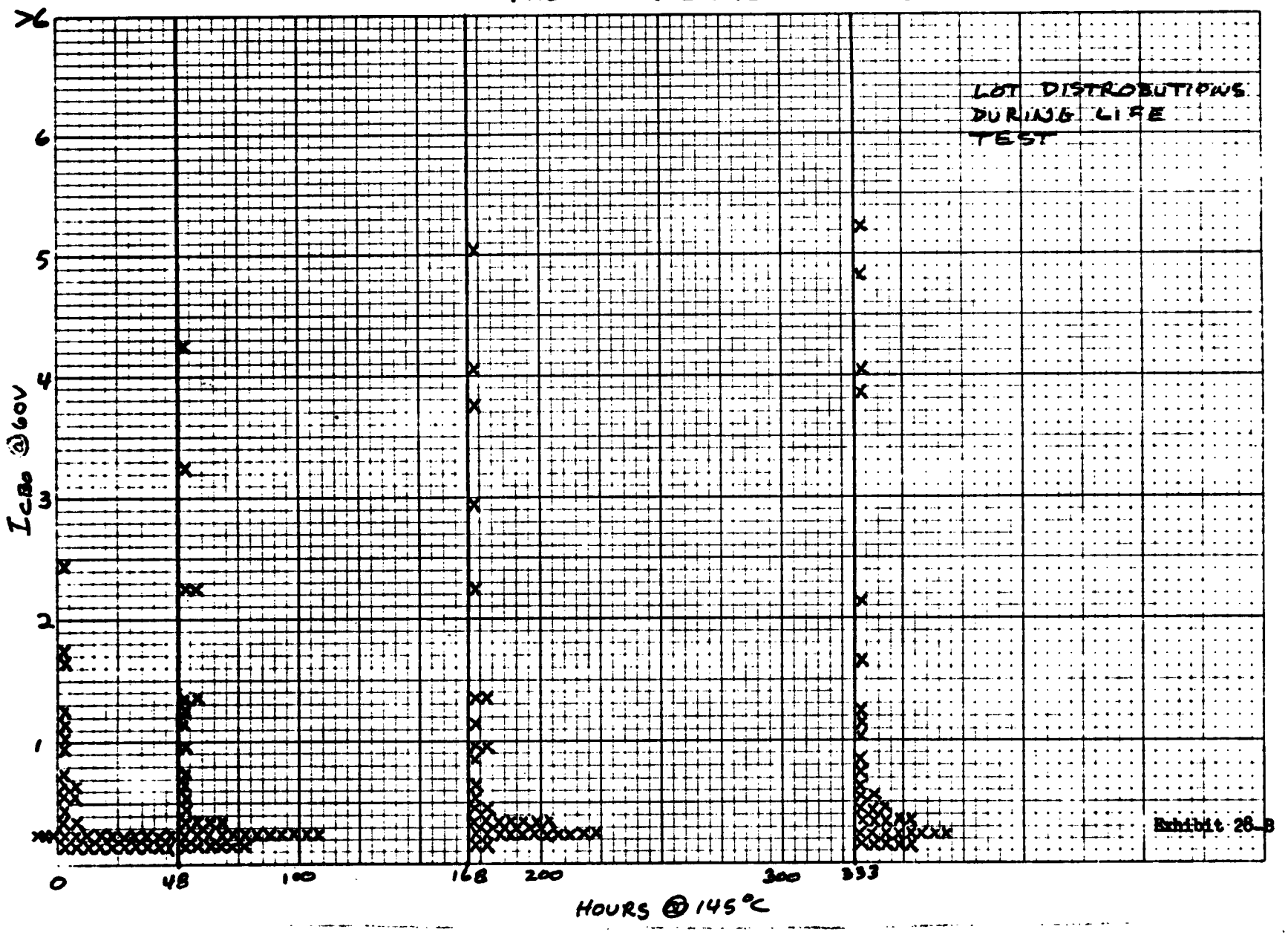

COMPARISON OF AVERAGE ICBO & IEBO VALUES FOR LOT WITH CALCIUM SULFATE AND LOT WITH MOLECULAR SIEVE PELLETS ON 145°C LIFE TEST.
CURRENT (MA)
3
2
1
I_{CBO} 60V – $CaSO_4$
I_{CBO} 60V – MOL. SIEVE
I_{EBO} 60V – $CaSO_4$
I_{EBO} 60V – MOL. SIEVE
Exhibit 27-A
0
48
100
168
200
300
333
400
HOURS @ 145°C


I_B (ma) @ I_C = 2a, V_{EB} = 2V
60
50
40
30
20
10
I_B – $CaSO_4$
I_C = 2a
I_B – Mol. Sieve
I_C = 2a
COMPARISON OF AVERAGE I_B VALUE FOR CALCIUM SULFATE VS. MOLECULAR SIEVE ON 146°C LIFE TEST.
Exhibit 27-E
0
16
100
168
200
300
333
400
HOURS @ 145°C

$CaSO_4$ - CONTROLS



MOLECULAR SIEVE PELLETS

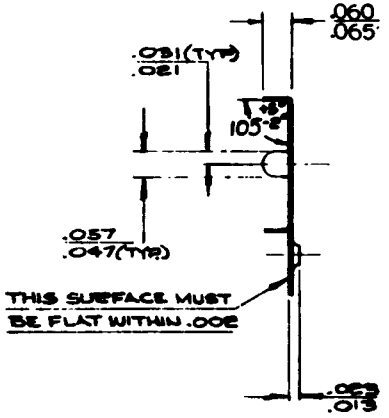


SIZE	DRAWING NO.	REV.
XB	45491	A

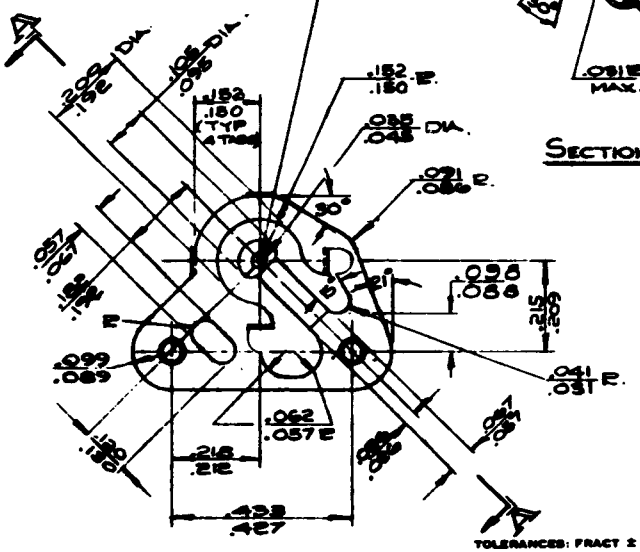
DIMENSIONS IN INCHES—DO NOT SCALE—PRINT

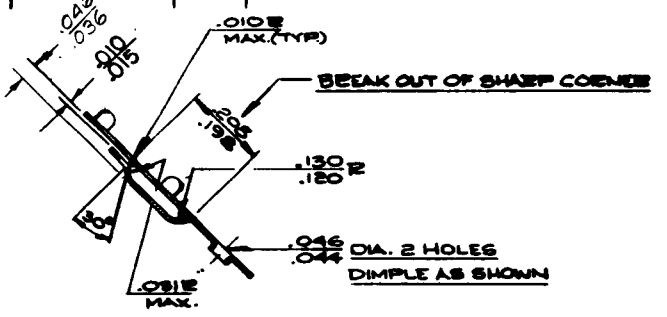
ITEM NO.	DRAWING NO.	NO. REQ'D.	DESCRIPTION

ACTUAL SIZE



CENTER OF TAB TO BE WITHIN .004 OF CENTER OF .152/.150 Ø





SECTION 'A-A'

TIP OF CENTRAL TAB (EMITTER TAB) SHALL BE FLAT AND PARALLEL WITH PLANE OF BODY WITHIN ±.005

REMOVE ALL BURRS & SHARP EDGES

TOLERANCES: FRACT ± 1/64 DEC ± .008 ANGLE ± ½° UNLESS OTHERWISE SPECIFIED

REV. LETR.	CH. NO.	REVISION	APPD.
A	5038	9/6/62	

MATL .0063 x ½ BEARS ¼ HARD (70-30)

2-21-61 DRAWN BY B.A.A.

CH'K'D BY

ENG. APPD.

MFG. APPD.

ISSUED

CLEVITE TRANSISTOR
A DIVISION OF CLEVITE CORPORATION
WALTHAM 54, MASS.

TITLE
2-6 CLIP (4 THD)
.040 DIA TERMINAL
FIRST USED ON 2-6 POWER TRANSISTOR

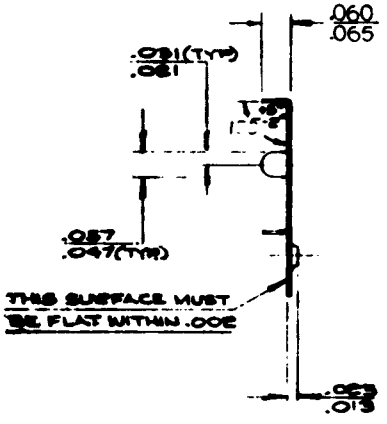
SCALE	SIZE	DWG NO.	REV.
4×1	XB	45491 EXH. 29	A

45501

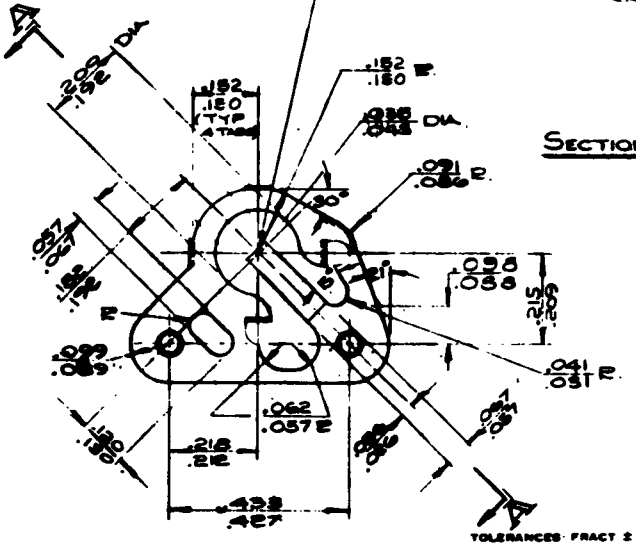
DIMENSIONS IN INCHES—DO NOT SCALE—PRINT

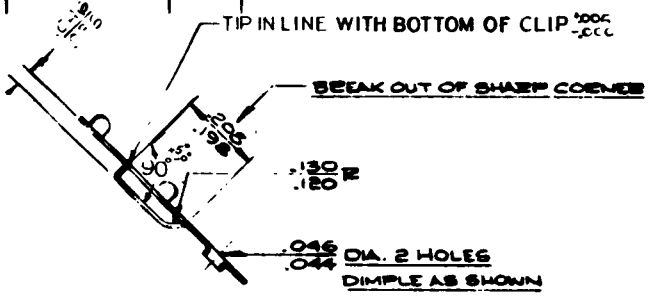
ITEM NO.	DRAWING NO	NO. REQ'D.	DESCRIPTION

ACTUAL SIZE



CENTER OF TAB TO BE WITHIN .004 OF CENTER OF .152/.150 Ⓔ





SECTION 'A-A'

TIP OF CENTRAL TAB (EMITTER TAB) SHALL BE FLAT AND PARALLEL WITH PLANE OF BODY WITHIN ±.005

REMOVE ALL BURRS & SHARP EDGES

TOLERANCES: FRACT ± 1/64 DEC ± .005 ANGLE ± ½° UNLESS OTHERWISE SPECIFIED

MAT'L .0068 × ½ BRASS ½ HARD (70-30)

2-21-61 DRAWN BY B.A.A.

CH'K'D BY

ENG. APPD.

MFG. APPD.

ISSUED

CLEVITE TRANSISTOR
A DIVISION OF CLEVITE CORPORATION
WALTHAM 54, MASS.

TITLE
E-6 CLIP (4 THS)
.040 DIA TERMINAL
FIRST USED ON E-6 POWER TRANSISTOR

SCALE 4×1 | SIZE XB | DWG NO. 45501 EXH 30 | REV.

REVISION | DATE | APPD

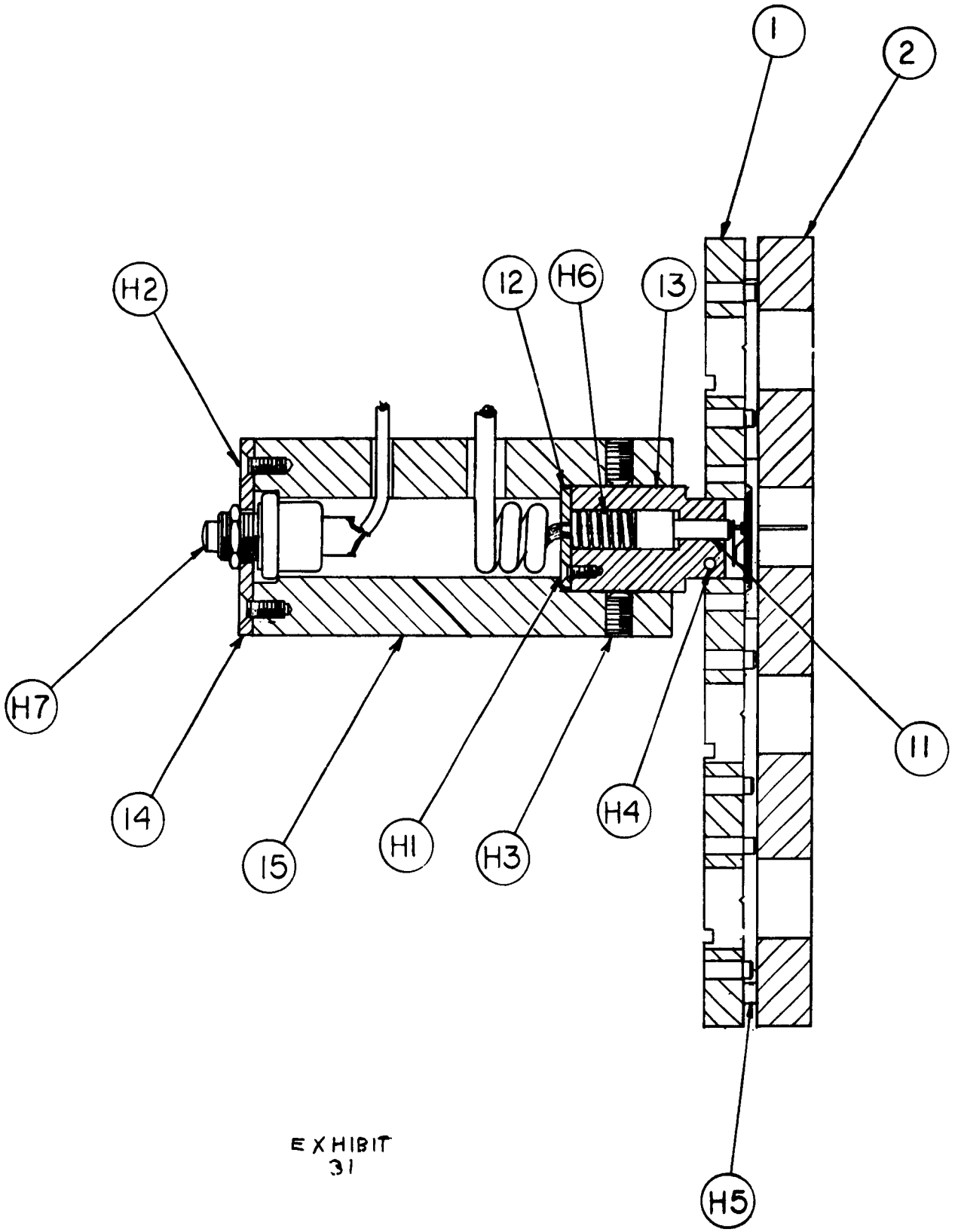
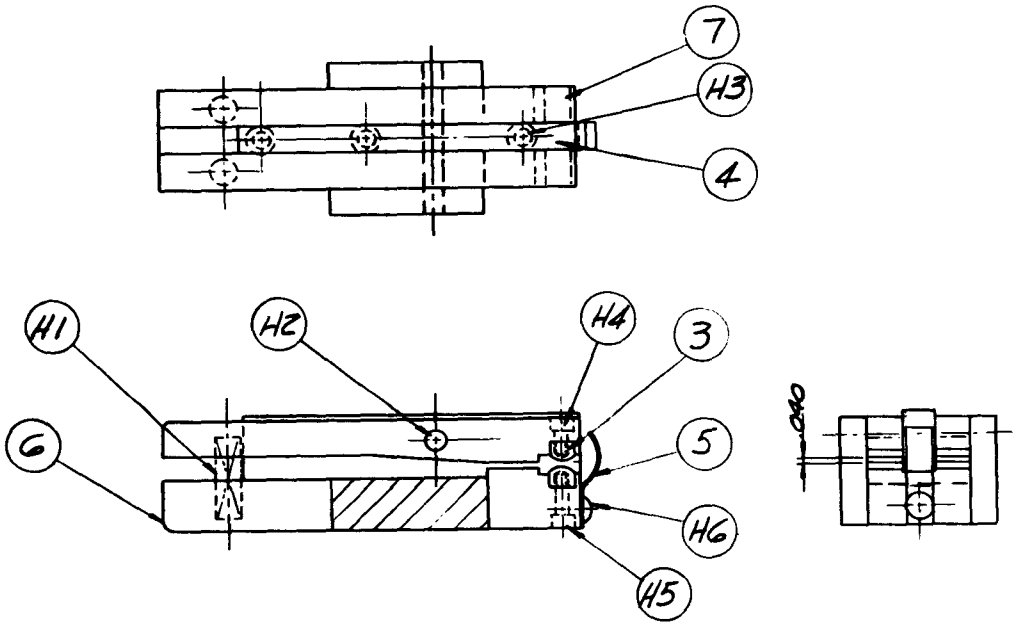


EXHIBIT
31

B 45844-01 A3M

DIMENSIONS IN INCHES—DO NOT SCALE—PRINT

ITEM NO.	DRAWING NO.	NO. REQ'D.	DESCRIPTION



TOLERANCES: FRACT ± 1/64 DEC ± .005 ANGLE ± ½° UNLESS OTHERWISE SPECIFIED

REV. LTR.	CH NO.	REVISION	APPD

MAT'L H

DRAWN BY RHB 1-10-63

CH'K'D BY

ENG. APPD.

MFG. APPD.

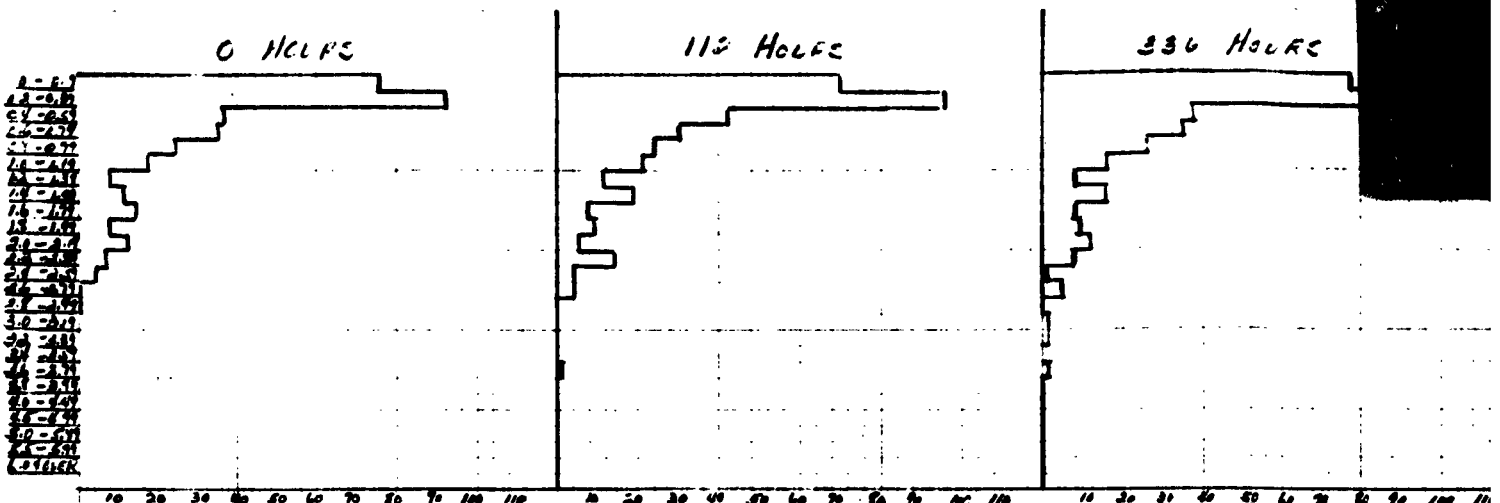
ISSUED 1-18-63

CLEVITE TRANSISTOR
A DIVISION OF CLEVITE CORPORATION
WALTHAM 54, MASS.

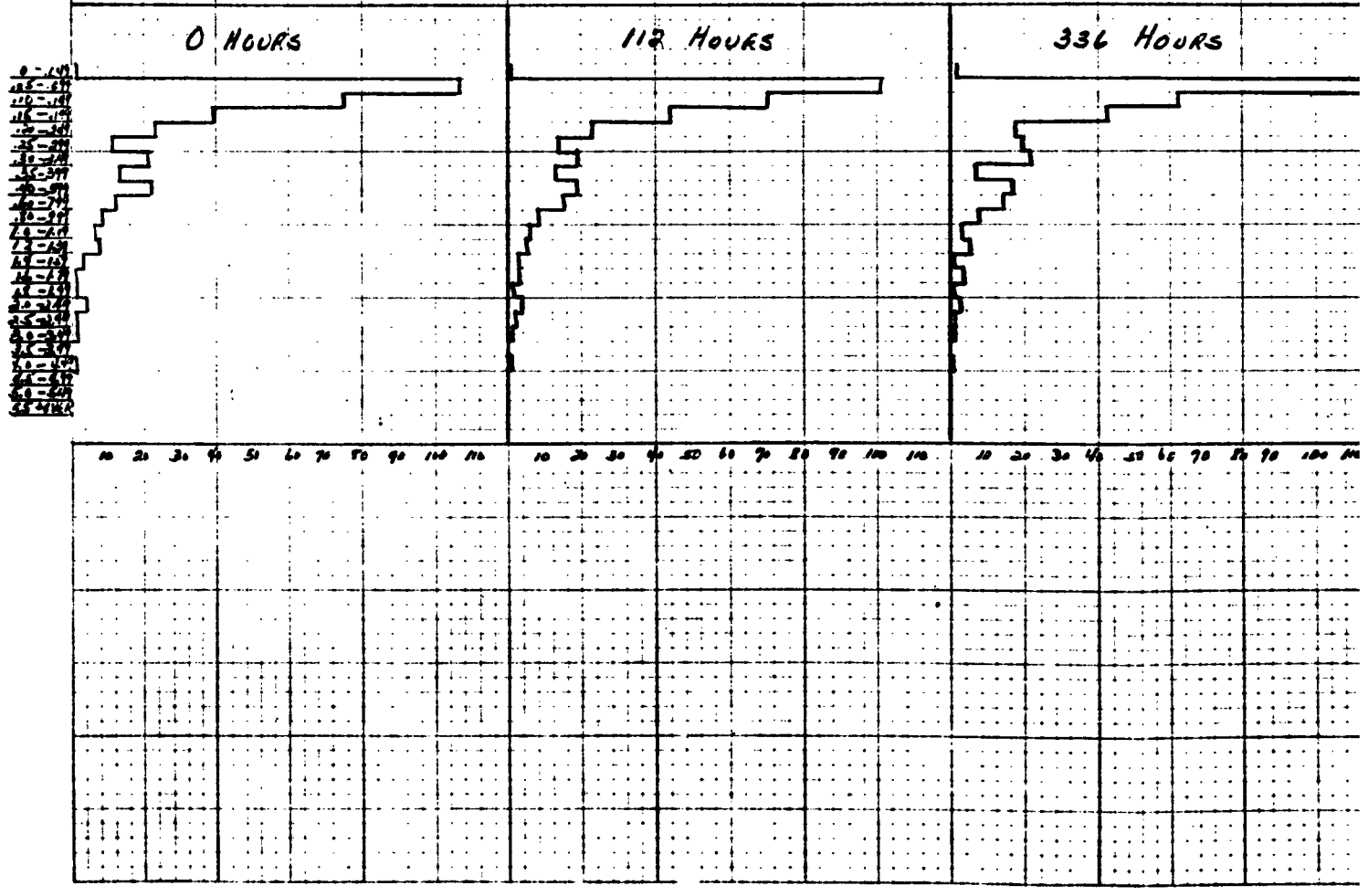
TITLE
TEST CONTACT HOLDER
TRANSISTOR HOLDER FOR TEST & BLOWOUT
FIRST USED ON 45844

SCALE	SIZE	DWG NO	REV.
FULL	B	45844-01	A

E 24-32



IEBO @ VEB = -60V 95°C STORAGE



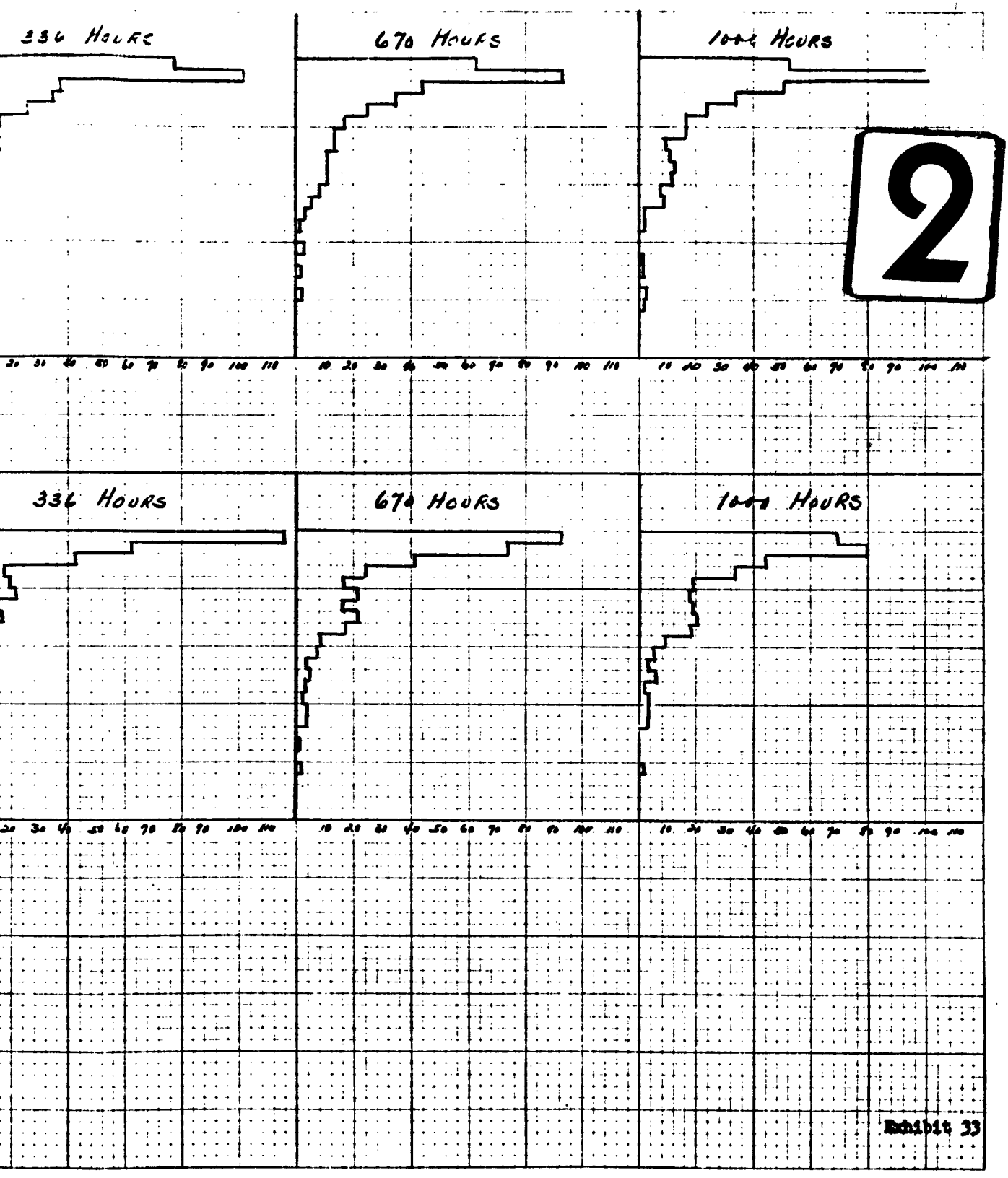
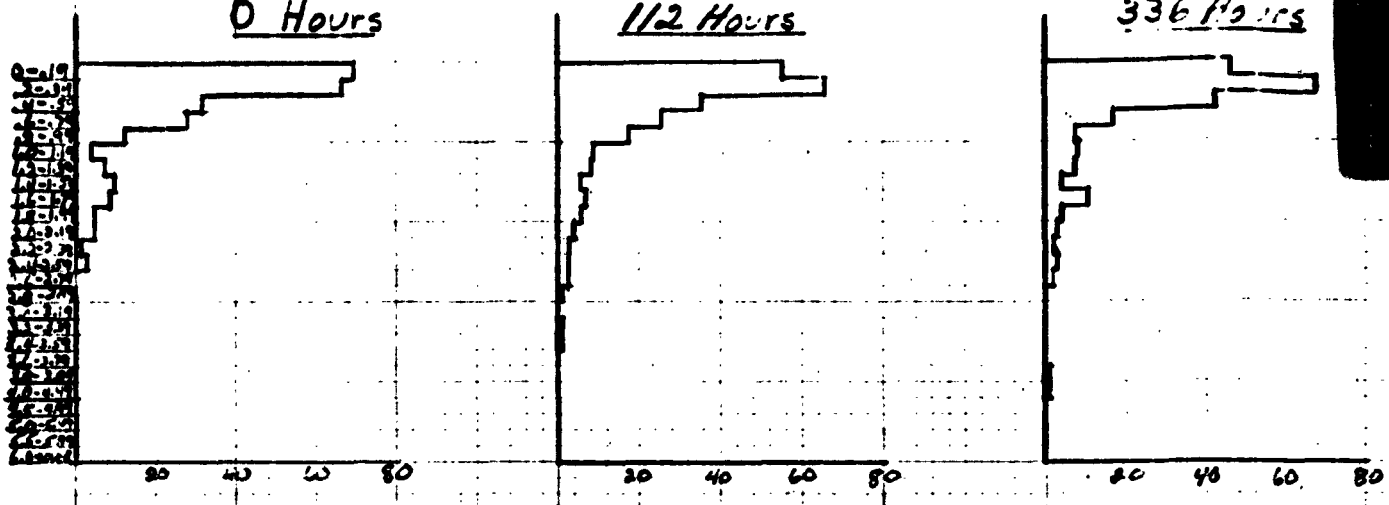
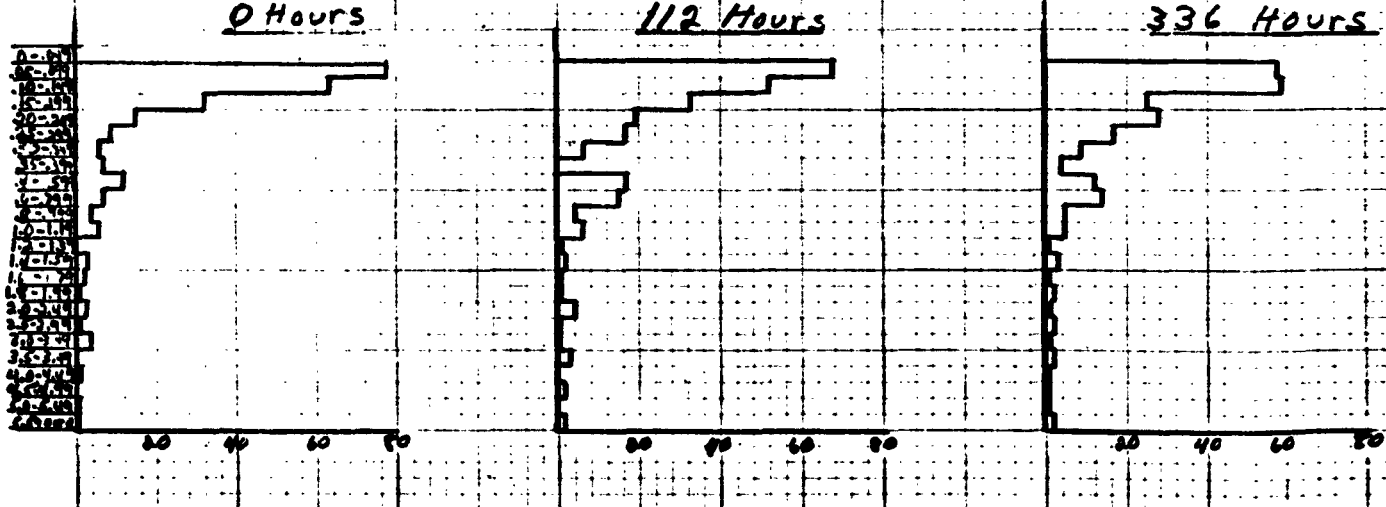

336 HOURS
670 HOURS
1004 HOURS
2
336 HOURS
670 HOURS
1004 HOURS

Exhibit 33

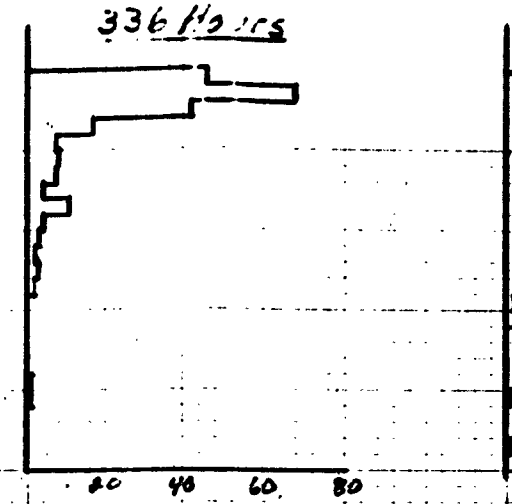
ICBO @ VCB = 10V. 125°C STORAGE



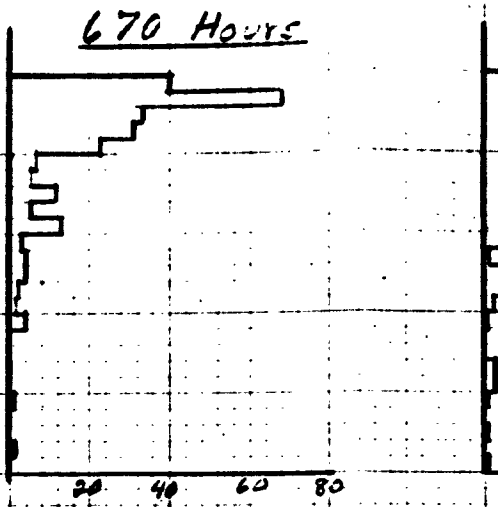
IEBO @ VEB = 60V. 125°C STorage



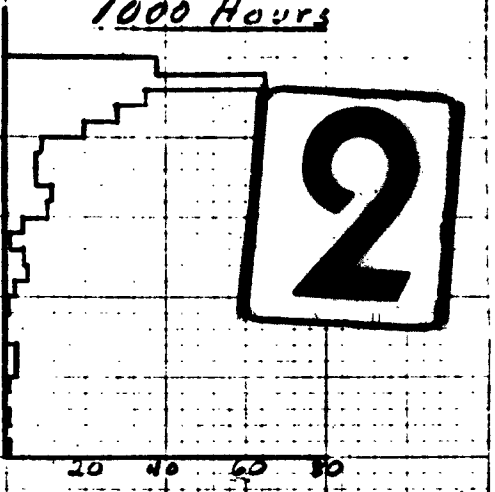
336 Hours



670 Hours

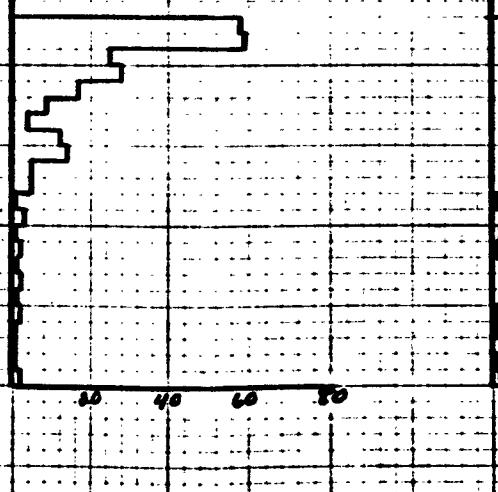


1000 Hours

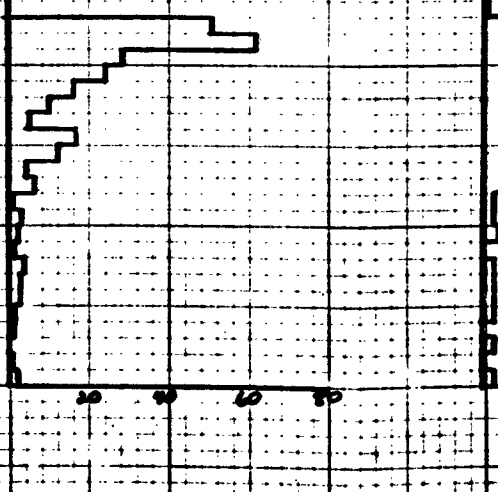


orage

336 Hours



670 Hours



1000 Hours

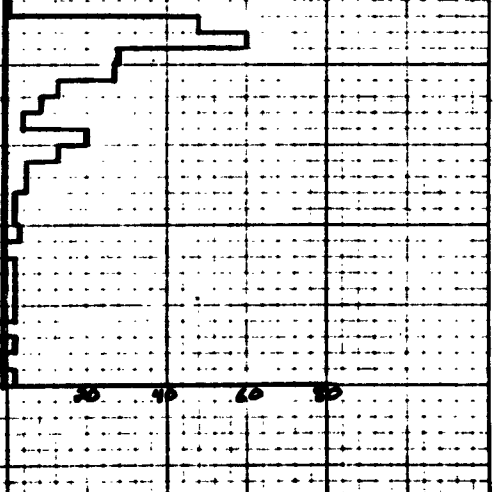
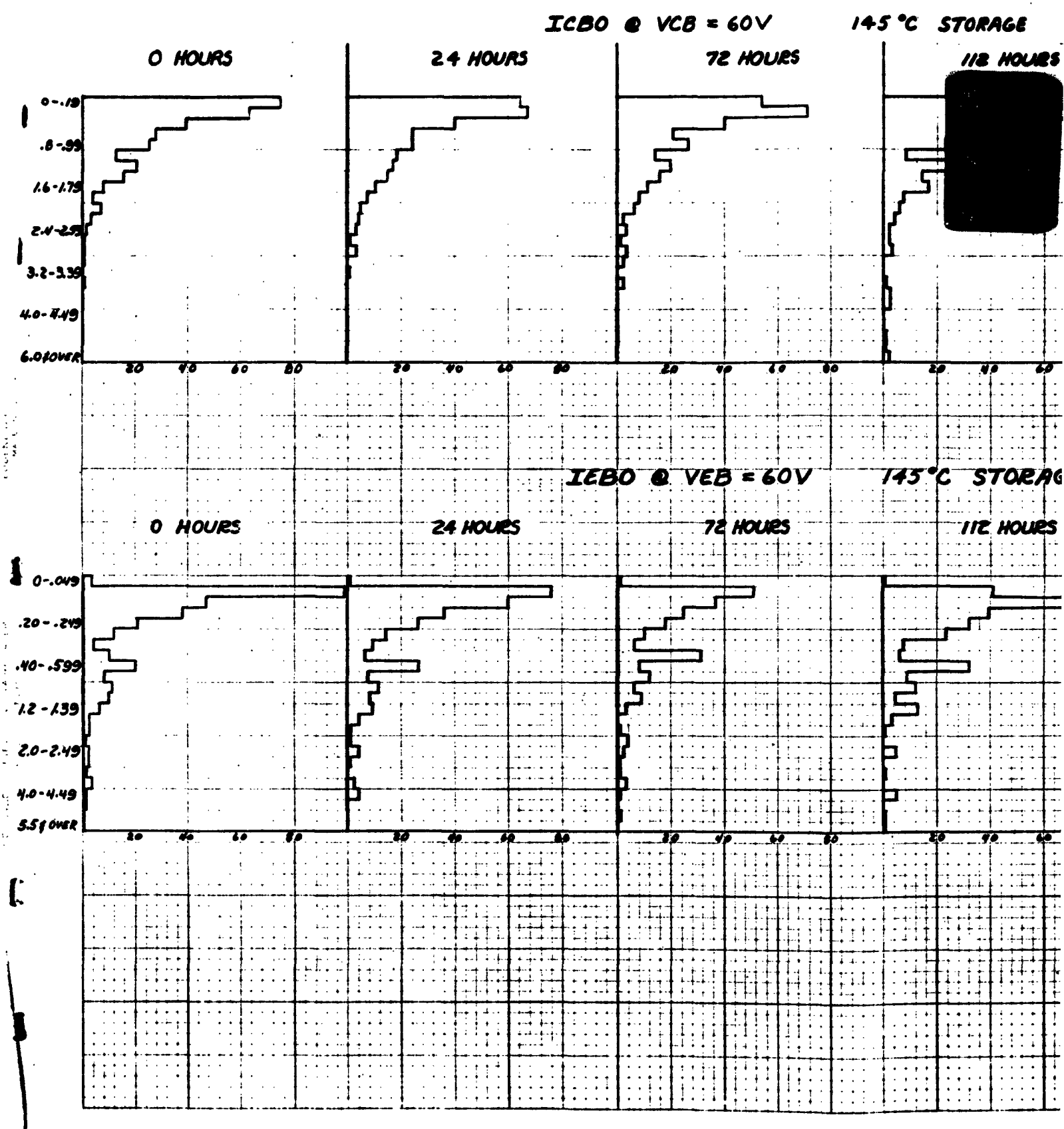


Exhibit 34


ICBO @ VCB = 60V
145 °C STORAGE
0 HOURS
24 HOURS
72 HOURS
112 HOURS
0-.19
.8-.99
1.6-1.79
2.4-2.59
3.2-3.39
4.0-4.19
6.0 & OVER
20
40
60
80
IEBO @ VEB = 60V
145 °C STORAG
0 HOURS
24 HOURS
72 HOURS
112 HOURS
0-.049
.20-.249
.40-.599
1.2-1.39
2.0-2.49
4.0-4.49
5.5 & OVER
20
40
60
80

'B = 60V 145 °C STORAGE

72 HOURS

112 HOURS

224 HOURS

336 HOURS

2

VEB = 60V 145 °C STORAGE

72 HOURS

112 HOURS

224 HOURS

336 HOURS

Exhibit 35

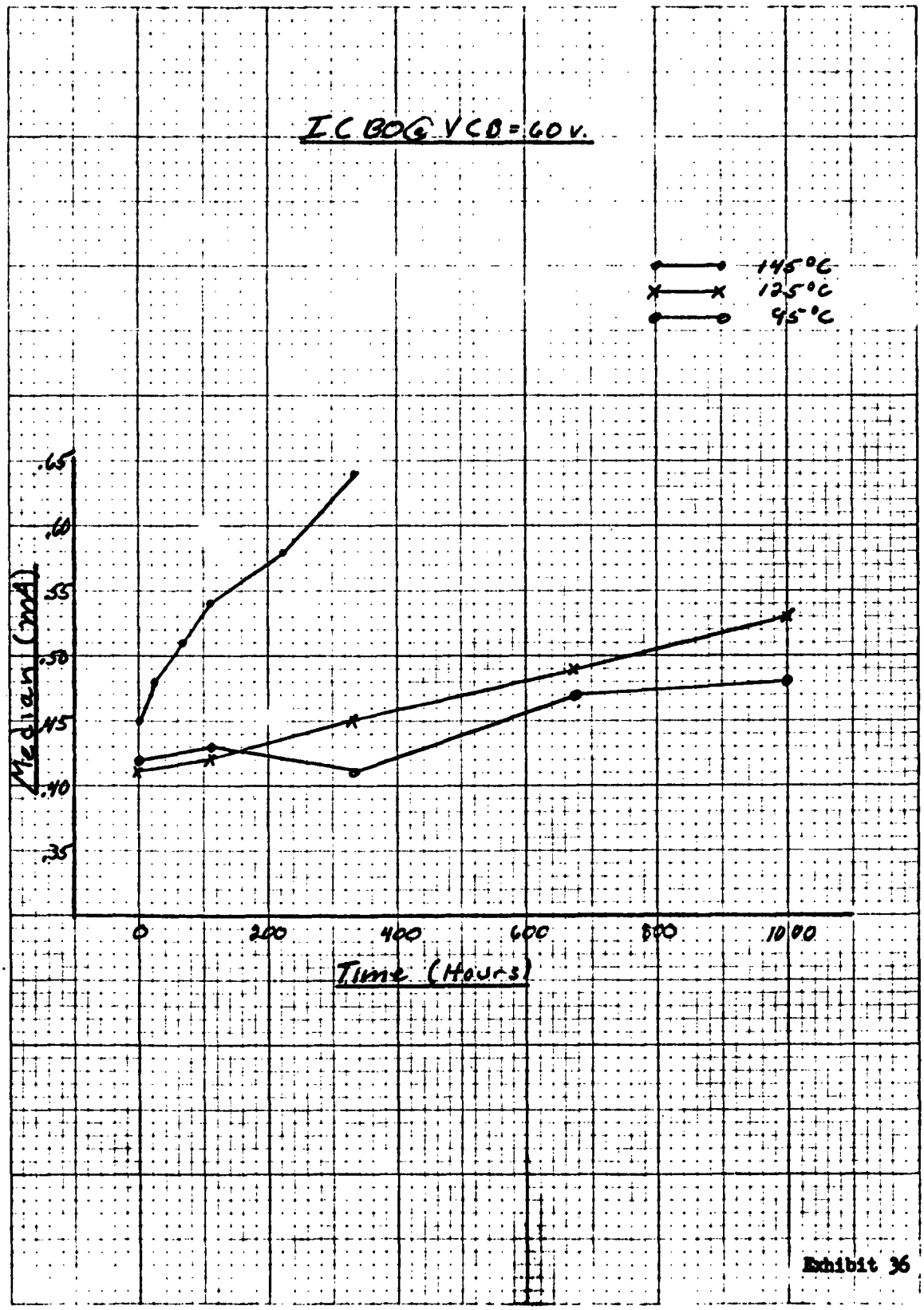

I C B O @ V C B = 60 V.
145°C
125°C
95°C
Median (mA)
.65
.60
.55
.50
.45
.40
.35
0
200
400
600
800
1000
Time (Hours)

Exhibit 36

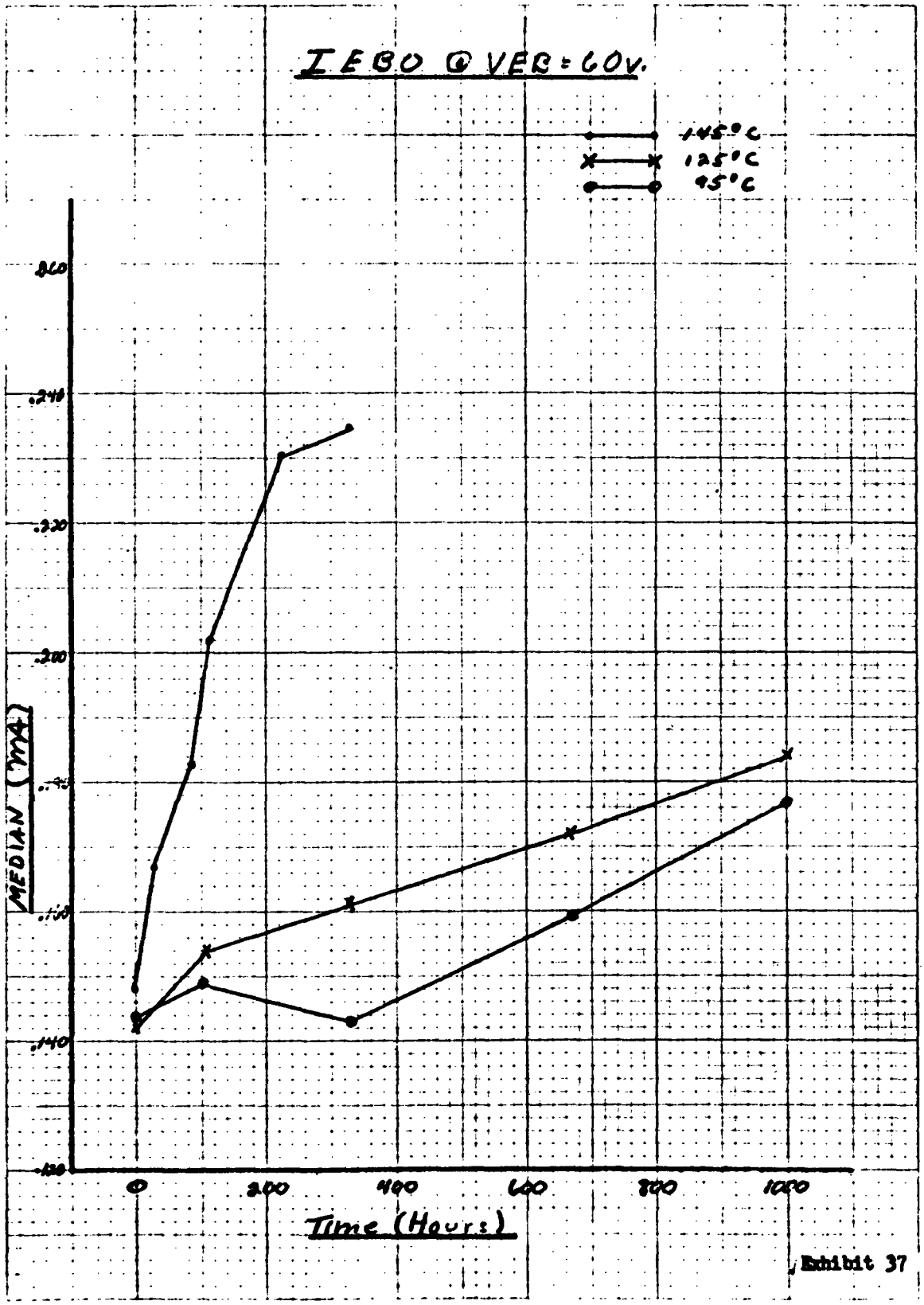
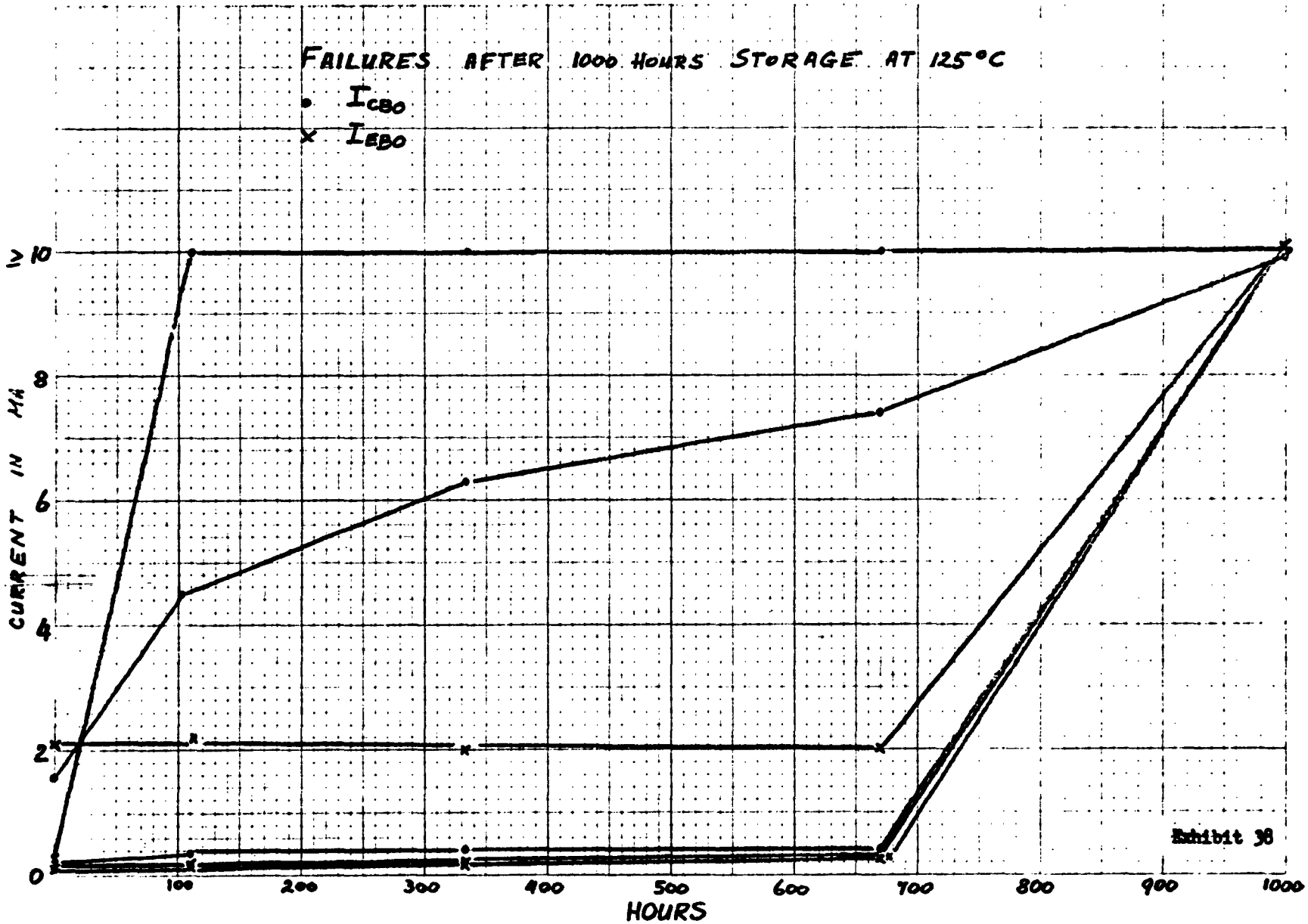
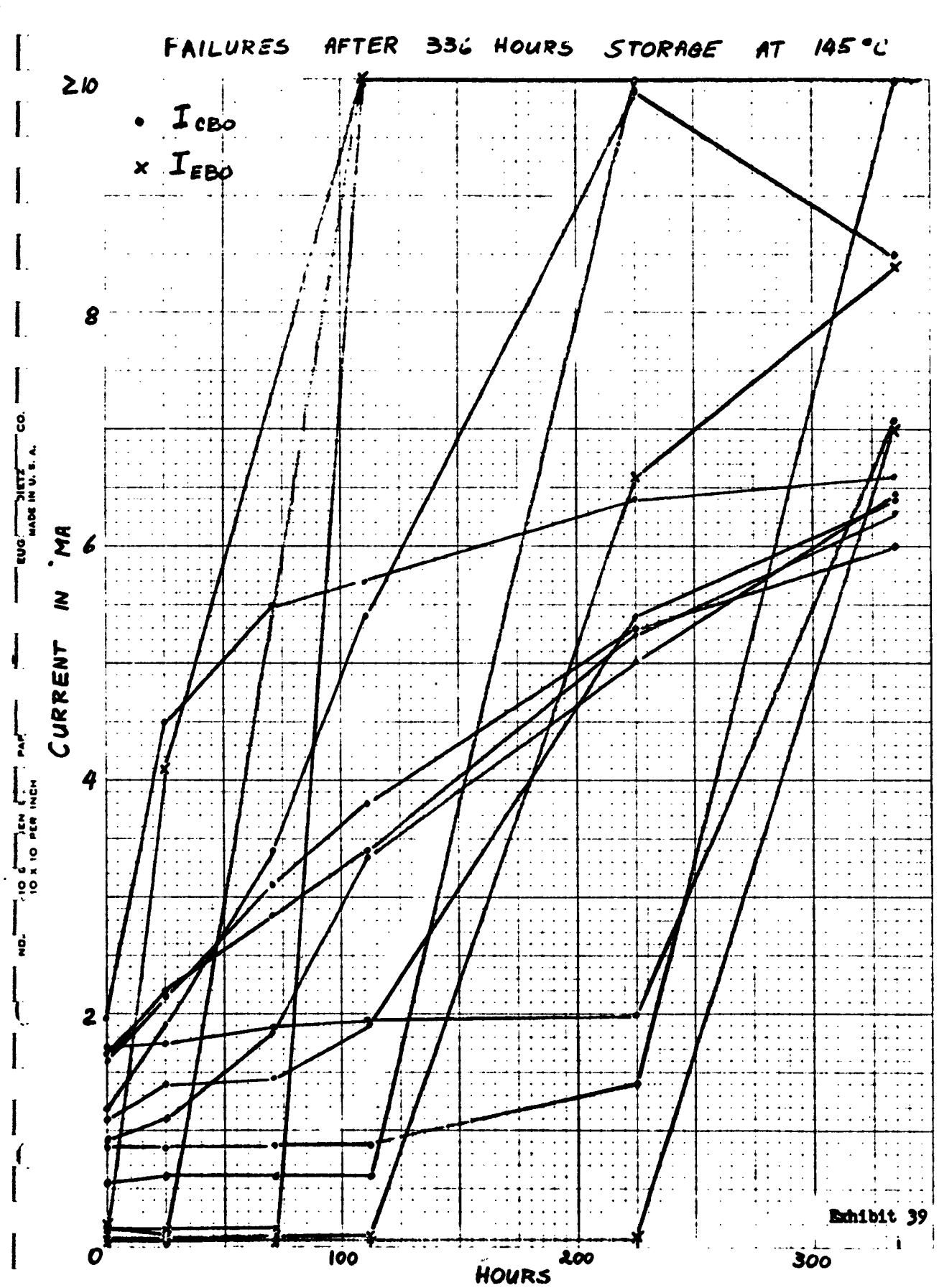


Exhibit 37


FAILURES AFTER 1000 HOURS STORAGE AT 125°C
• I_{CBO}
× I_{EBO}
CURRENT IN MA
0
2
4
6
8
10
100
200
300
400
500
600
700
800
900
1000
HOURS
Exhibit 38


FAILURES AFTER 336 HOURS STORAGE AT 145°C
• I_{CBO}
× I_{EBO}
CURRENT IN MA
HOURS
0
2
4
6
8
10
100
200
300
Exhibit 39

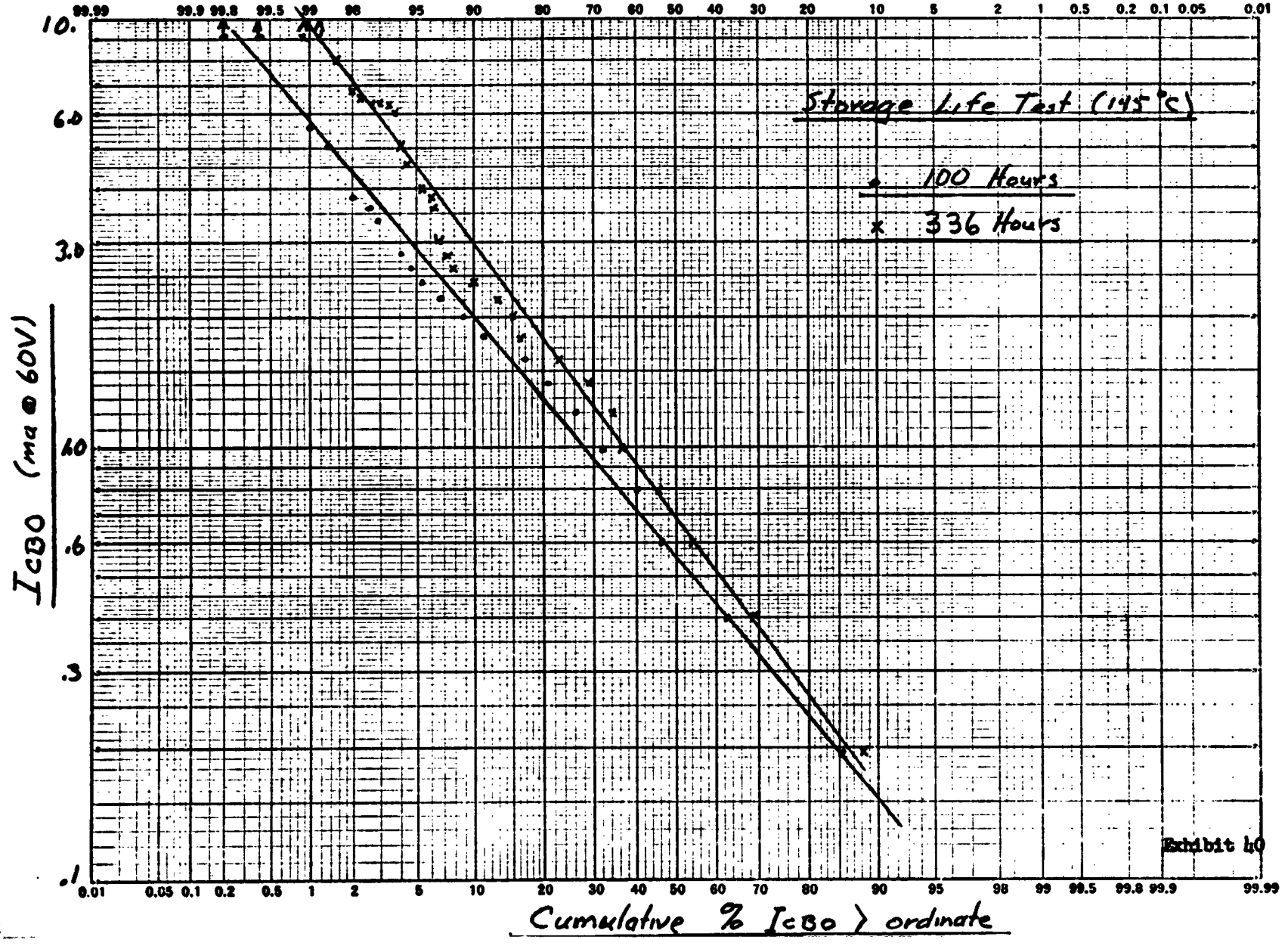


Exhibit 40

RE-ETCHED STORAGE LIFE UNITS.

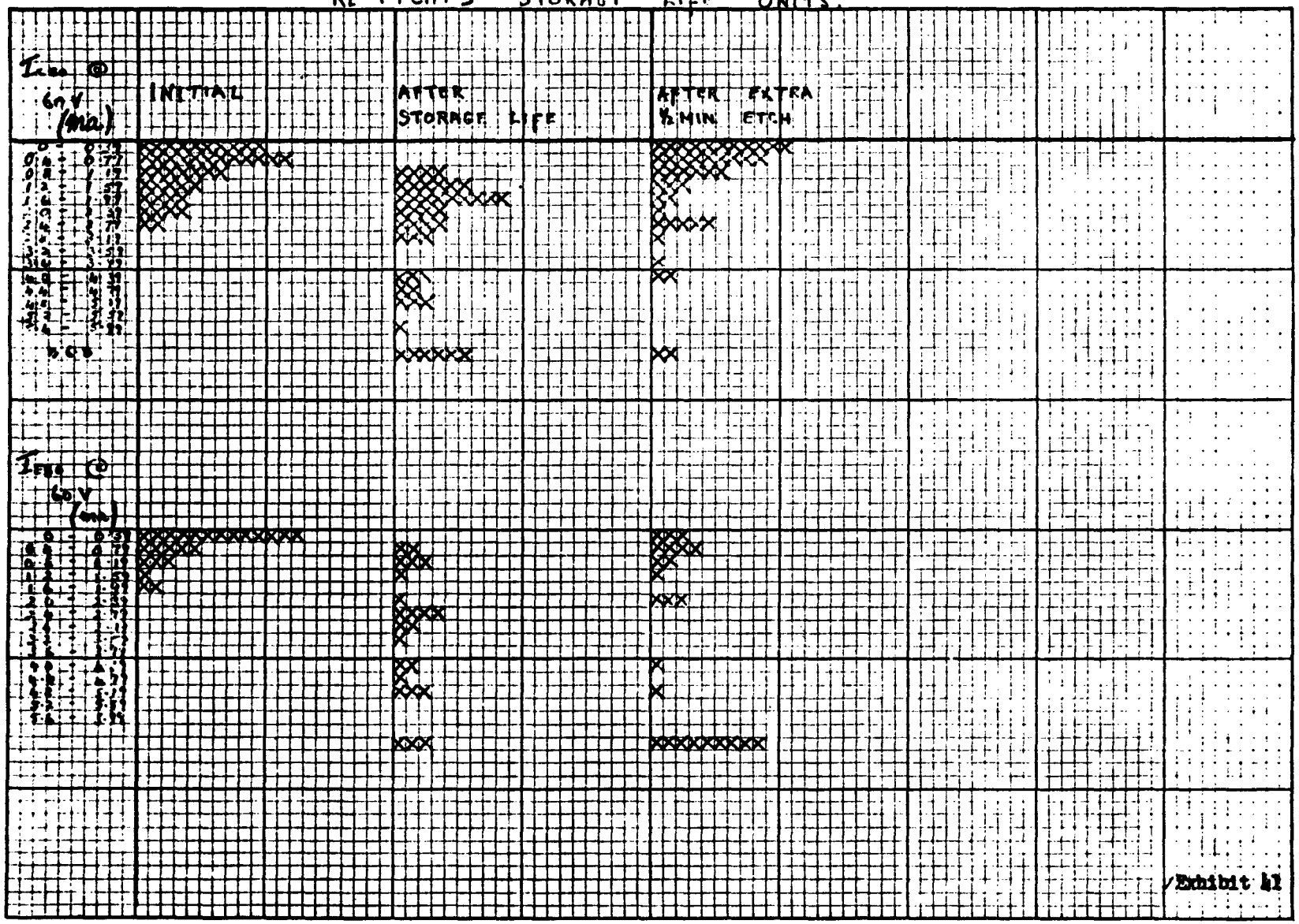


Exhibit 42

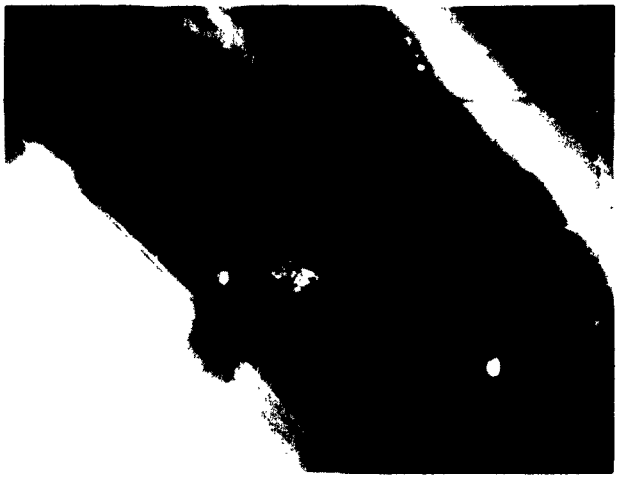
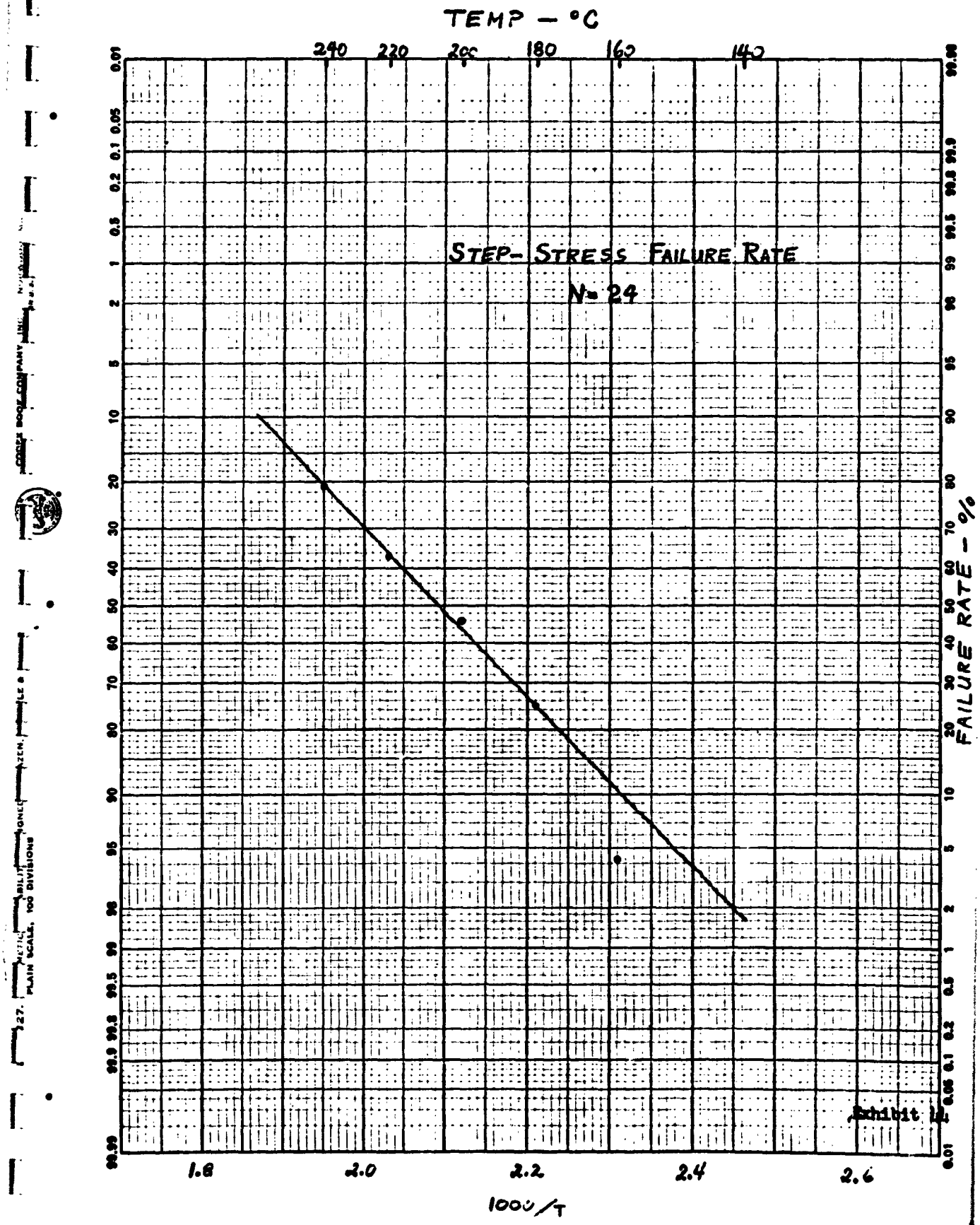


Exhibit 43


TEMP — °C
240
220
200
180
160
140
STEP-STRESS FAILURE RATE
N= 24
FAILURE RATE — %
1.8
2.0
2.2
2.4
2.6
1000/T
Exhibit 12